SERVICE MANUAL

PT - 200 CHASSIS

Modification reserved

CONTENTS

RECOMMENDATION FOR SERVICE REPAIRS

1- Use only original spare parts. Only use components with the same specifications for replacement.
2- Original fuse value only should be used.
3- Main leads and connecting leads should be checked for external damage before connection.
Check the insulation.
4- Parts contributing to the safety of the product must not be damaged or obviously unsuitable.
This is valid especially for insulators and insulating parts.
5- Thermally loaded solder pads are to be sucked off and re-soldered.
6- Ensure that the ventilation slots are not obstructed.
7- Potentials as high as 31 KV are present when this receiver is operating. Operation of the receiver outside the cabinet or with back cover removed involve a shock hazard from the receiver.
Servicing should not be attempted by anyone who is not thoroughly familiar with the precautions necessary when working on high voltage equipment.
Perfectly discharge the high potential of the picture tube before handling the tube. The picture tube is highly evacuated and if broken.
Glass fragments will be violently expelled.
Always discharge the picture tube anode to the receiver chassis to keep of the shock hazard before removing the anode cap.
8- Keep wire away from the high voltage or high temperature components.
9- When replacing a wattage resistor in circuit board, keep the resistor 10 mm away from circuit board.
10) Discharging of the picture tube is effected only by the connection point of the aquadaq coating the picture tube.
11) When carrying out repairing process at control unit do not approach too near to the picture tube in order to avoid any charge transfer.
12) Measurements within the primary circuit of the switched mode power supply are allowed to be carried out only when using potential-free measuring equipment. Voltages indicated for this circuit are based on mains voltage reference level.
13) The defined local radiation dosage according to the x-ray radiation regulation is given by the specific type of the picture tube and the maximum permissible EHT voltage. The EHT voltage must not exceed the maximum value of 31kv.
14) When the repair process is carried out 12 V line voltage should not be interrupted because video output stage is endangered by the interruption of 12 V line voltage.

HANDLING OF MOS CHIP COMPONENTS

MOS circuit requires special attention with regard to static charges. Static charges may occur with any highly insulating plastics and can be transferred to persons wearing clothes and shoes made of synthetic materials. Protective circuits on the inputs and outputs of mos circuits give protection to a limited extend only due to time of reaction.

Please observe the following instructions to protect the components against damage from static charges.

1- Keep mos components in conductive package until they are used. Most components must never be stored in styropor materials or plastic magazines.
2- Persons have to rid themselves of electrostatic charges by touching MOS components.
3- Hold the component by the body touching the terminals.
4- Use only grounded instruments for testing and processing purposes.
5- Remove or connect MOS ICs when operating voltage is disconnected.

X-RAY RADIATION PRECAUTION

1- Excessive high voltage can be produce potentially hazardous X-RAY radiation. To avoid such hazard, the high voltage must not be above the specified limit. The value of the high voltage of this receiver is 30KV at zero beam current (minimum brightness) under 220V AC power source. The high voltage must not under any circumstance, exceed 31.5KV. It is recommended the reading of the high voltage be recorded as a part of the service record. It is important to use an accurate and reliable high voltage meter.

2- The primary source of X-RAY radiation in this TV receiver is the picture tube. For continued X-RAY radiation protection, the replacement tube must be exactly the same type tube as specified in the part list.

SOLDERING PROCESS

1) SMD Components (Surface Mounted Device)

Desoldering:

Heat up the component from its terminals for 2 or 3 seconds with a soldering iron and afterwards take out the component carefully by means of the tweezers. Remove superfluous solder at the solder surfaces of the components place at pcb by means of desoldering strand or suction de-solder equipment. Never force the component for removing without heating the terminals sufficiently. Unsoldered components should not be used for once more.

Soldering:

Place the component properly to its position by means of tweezers and solder one side of the component. Then check out the position of the component and be sure if it is soldered to the right place and then solder other side of the component. Terminals of the SMD components must not contact directly to the soldering iron.

2)PLCC Components

Desoldering:

Heat up the terminals of PLCC component for 3 or 5 seconds by means of SMD soldering iron and PLCC desoldering pair (angle 90°C, Leg: 24mm). Take out PLCC component carefully by slightly turning of desoldering tweezers.

Soldering:

Remove superfluous solder at the solder surfaces of the components placed on pcb by means of de-soldering iron or suction de-solder equipment. Apply flux with low grease content. Place PLCC device on the soldering surface and take care for its correct placement. Secure diagonally by means of two soldering joints. Apply soldering paste along PLCC pins. Short circuits which may occure during soldering process have to be removed immediately with a soldering iron.

EURO SCART

I- Audio output 1. right channel 0.5 VRMS/<I k 0

2- Audio input 1. right channel 0.5 VRMS (connected to No.6)

3- Audio output 2. left channel 0.5 VRMS (connected to No.1)

4- GND (audio)

5- GND

6- Audio input 2. left channel 0.5 VRMS/>10k 0

7- RGB input, blue (B)

8- Switch signal video (status)

9- GND

10- Reserved for clock signals (not connected)

11- RGB input, green (G)

12- Reserved for remote control (not connected)

13- GND

14- GND switch signal RGB

15- RGB input, red (R)

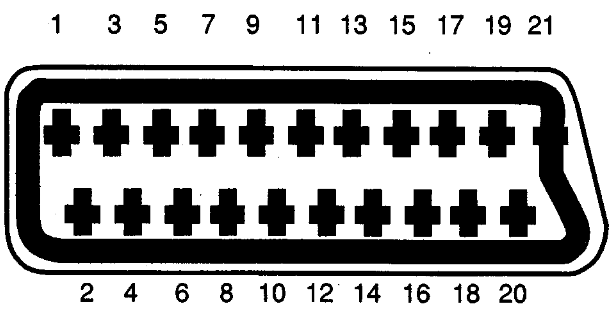
16- Switch signal RGB

17- GND (video)

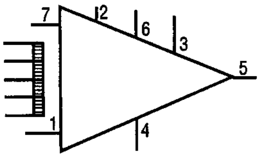
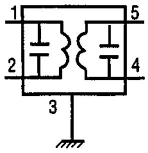
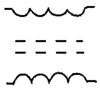
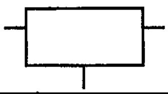
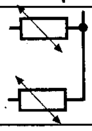
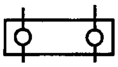
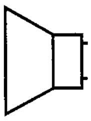
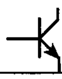
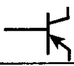
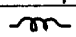
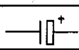
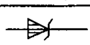
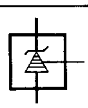
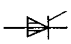
18- GND19- Video output 1 Vpp/75 ohm

20- Video input 1 Vpp/75 ohm

21- Shield



COMPONENT DESCRIPTIONS

	POWER AMPLIFIER
	SAW FILTER
	LINE FILTER
	VOLTAGE REGULATOR
	PTC
	CONNECTOR
	LOUD-SPEAKER
	NPN TRANSISTOR
	PNP TRANSISTOR
	COIL
	LINEARITY COIL
	CERAMIC FILTER
	RESISTOR
	CERAMIC CAPACITOR /POLYESTER CAPACITOR
	ELECTROLYTIC CAPACITOR
	DIODE
	ZENER DIODE
	PROGRAMMABLE VOLTAGE REFERENCE
	THYRISTOR

TECHNICAL DATA SHEET

CHASSIS		PT200
	Consept	ST CTV 100 (32 bit technology)
PICTURE		
	Picture tube diagonal / format /Deflection	28" 4:3 /29" TF 4:3 110" 28"/32" 16/9 SF/TF106"
	Format	4:3 sets: Cinema, Centeral, 16:9, Auto 16:9 sets: 16:9, 4:3, Cinema, Panoramic, Zoom, Auto
	Digital Colour Transition Improvement	•
	Comb Filter	•
	Noise Reduction	•
	Flicker Reduction	•
	Dynamic Adaptive Peaking	•
	Global Motion Detection / Compensation	•
	Scan Velocity Modulation	°
	Freeze	•
TUNING		
	Tuner	PLL
TV Systems	PAL / SECAM / BG / BG DK / I / LL"	•/•/•/•/•
	NTSC 4.43MHz Playback	•
	NTSC 3.58MHz Playback	•
Channel coverage	VHF / UHF	•
	CATV / Hyperband (S1-S41)	•
	Auto Programming	•
	ATS Euro Plus tuning system	•
	Fine-tuning	•
	Program storage capacity	200
TELETEXT		
	Top text / Fast text	• / •
Teletext memory	2048 page	•
	Text capability in OSD Languages	•
GENERAL FEATURES		
	OSD Menu in multi languages	Turkish, English, German, Dutch, Czech, Polish
	Available Cabinets	28" 4:3 : Aura, Terra, NewCroma, Mira, Mega 28"/32" 16:9 : Nova, Croma, Prima, Trueflat 28" 16:9 : Aura, Terra
	Sleep timer	•
	Auto shut-off	•
	Child Lock	•
	Program naming	•
	Swap function (Recall)	•

	Timer controlled program switching (on-timer)	•
	Transparent OSD	•
	Mutipicture mosaic	• (16 picture)
	PAT (Picture & teletext)	•
	PIT (Picture in Teletext)	•
	PIP w / double tuner	○
	3 size / 4 position / swap features for PIP	•
	2PAT (2 pictures & teletext) (A/V w/ PIP d.tuner)	○
SOUND		
	A2 + Nicam stereo	•
	Auto Volume Control(AVC)	•
	Sound Effect (Wide sim.)	•
	5 band graphic equalizer	•
	5 preset sound modes	• (flat, hall, music, movie, personal)
	Balance	•
	Audio output power (rms)	2 * 6 W (10%THD)
POWER SUPPLY		
	Operating Voltage (165-265 Vac / 50 Hz)	•
	Power consumption	28" / 29" 4:3, 28"/32" 16:9 135W
	Stand-by power consumption	< 3W
CONNECTIONS		
	Antenna input (75 ohm IEC)	•
	Euro-AV Scart (RGB + AV + SVHS(optional))	•
	Second Scart (AV only)	• (RGB optional)
	Third Scart (AV only)	○
	S-VHS din socket + Audio L/R Input	○
	2ch audio line out	○
	Side AV-IN	•
	Headphone Socket	•
ACCESSORIES		
	Remote control unit (Full function)	TM3602PT200
●: Standart	**○: optional.**	

SERVICE MENU AND BASIC ADJUSTMENTS

The procedure to enter the "SERVICE MODE" for PT200 and the setups in this mode are explained below:

1. ENTER THE SERVICE MODE

• When the main menu is on the screen , press the 1 9 2 3 numbers successively to enter the service mode.

2. SETUP MENU.

• OSD translucency.
• 4/3, 16/9.
• Teletext Languages.
• Tuner Selection.
• PIP tuner selection.
• Main tuner AGC.
• OSD Brightness.
• Teletext Brightness.
• OSD Color.
• Teletext Color.
• Scart3 Option
• SVHS Option.

3. Geometry.

• V – Slope.
• V – Position.
• V – Amplitude.
• V – S Correction.
• H – Blanking.
• H – Shift.
• EW – Width.
• EW – Pin – cushion.
• EW – Trapezium.
• EW – Upper corner.
• EW – Lower corner.
• H – Parallelogram.
• H – Bow
• EW – EHT Compens.
• Restore Default.

4. Video

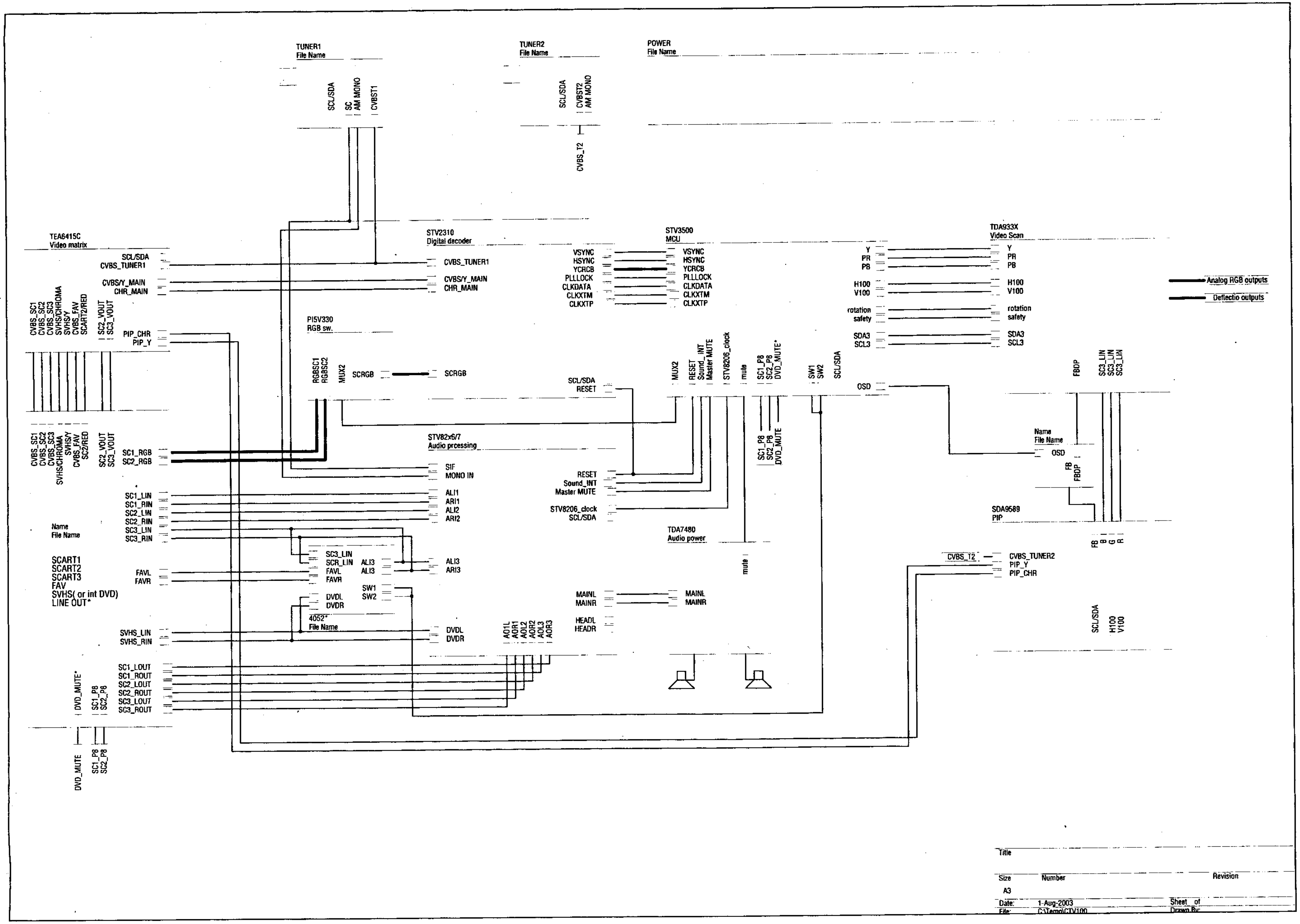
• G2 Aligment.
• White Point R.
• White Point G.
• White Point B.
• Peak White Limiter.
• Black level offset R.
• Black level offset G.
• Gain Pre – Scale RGB.
• Fast Blanking delay.
• Luma / Chroma delay.
• Restore Default.

5. Sound

• L / L' AGC Adj.
• PreScl SCART.
• PreScla FM
• Pre Scl NICAM
• Prescale MONO

6. Pip Service

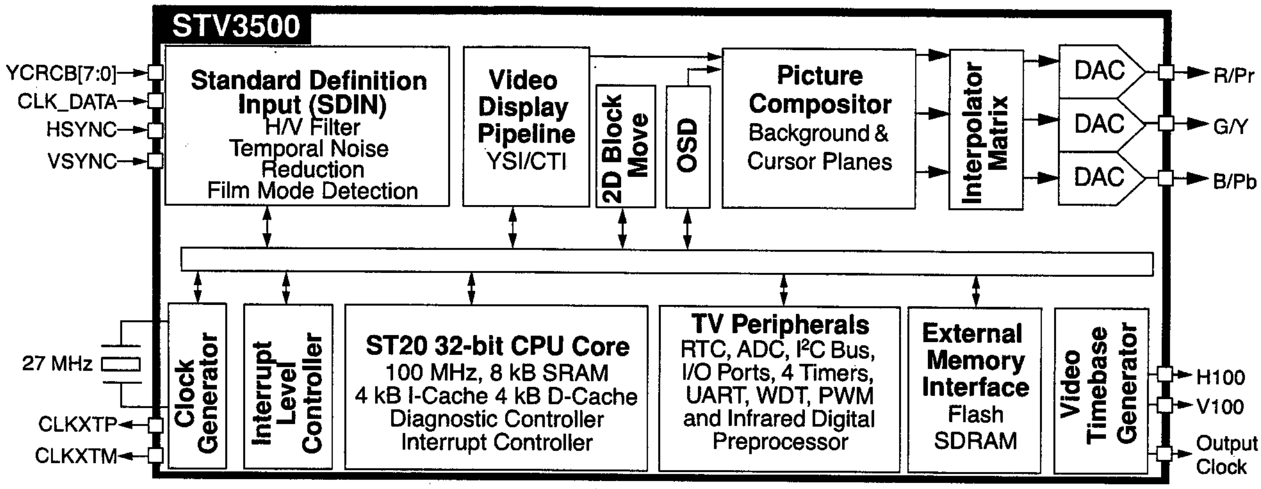
• Saturation.
• Frame Color.
• Frame Width V.
• Frame Width H.
• Contrast.
• Y / C Delay.
• Pip Tuner AGC.
• Pip IC AGC.


TUNER1
File Name
SCL/SDA
SC
AM MONO
CVBST1
TUNER2
File Name
SCL/SDA
CVBST2
AM MONO
CVBS_T2
POWER
File Name
TEA6415C
Video matrix
SCL/SDA
CVBS_TUNER1
CVBS/Y_MAIN
CHR_MAIN
CVBS_SC1
CVBS_SC2
CVBS_SC3
SVHS/CHROMA
SVHS/Y
CVBS_FAV
SCART2/RED
SC2_VOUT
SC3_VOUT
PIP_CHR
PIP_Y
SC1_RGB
SC2_RGB
STV2310
Digital decoder
CVBS_TUNER1
CVBS/Y_MAIN
CHR_MAIN
VSYNC
HSYNC
YCRCB
PLLLOCK
CLKDATA
CLKXTM
CLKXTP
SCL/SDA
RESET
PI5V330
RGB sw.
RGBSC1
RGBSC2
MUX2
SCRGB
STV3500
MCU
MUX2
RESET
Sound_INT
Master MUTE
STV8206_clock
mute
SC1_P8
SC2_P8
DVD_MUTE*
SW1
SW2
SCL/SDA
Y
PR
PB
H100
V100
rotation
safety
SDA3
SCL3
OSD
TDA933X
Video Scan
Analog RGB outputs
Deflectio outputs
FBDP
SC3_LIN
Name
File Name
OSD
FB
FBDP
SDA9589
PIP
FB
B
G
R
CVBS_T2
CVBS_TUNER2
PIP_Y
PIP_CHR
SCL/SDA
H100
V100
STV82x6/7
Audio prcessing
SIF
MONO IN
ALI1
ARI1
ALI2
ARI2
ALI3
ARI3
DVDL
DVDR
RESET
Sound_INT
Master MUTE
STV8206_clock
SCL/SDA
MAINL
MAINR
HEADL
HEADR
AO1L
AOR1
AOL2
AOR2
AOL3
AOR3
TDA7480
Audio power
mute
SC1_LIN
SC1_RIN
SC2_LIN
SC2_RIN
SC3_LIN
SC3_RIN
FAVL
FAVR
SVHS_LIN
SVHS_RIN
SC1_LOUT
SC1_ROUT
SC2_LOUT
SC2_ROUT
SC3_LOUT
SC3_ROUT
DVD_MUTE*
SC1_P8
SC2_P8
DVD_MUTE
Name
File Name
SCART1
SCART2
SCART3
FAV
SVHS(or int DVD)
LINE OUT*
SC3_LIN
SCR_LIN
FAVL
FAVR
ALI3
ALI3
SW1
SW2
DVDL
DVDR
4052*
File Name
Title
Size
Number
Revision
A3
Date: 1-Aug-2003
Sheet of
File: C:\Temp\CTV100
Drawn By:

13- DESCRIPTION OF INTEGRATED CIRCUITS

STV3500

Integrated Up-Converter with 32-bit CPU Core with Enhancers and Bitmap On-Screen Display



Main Features

Versatile Integrated Up-Converter

- 100/120-Hz Interlaced: AABB, AA*B*B, AA*BB*, ABAB or AAAA Field-Repeat
- Motion Driven 100-Hz Up-conversion based on Median Filter
- 50/60-Hz Progressive with Line-Interpolation, Field-Merging with Motion-adaptive De-interlacing
- Advanced Still Picture modes: AA*AA* and ABAB interlaced or AAAA non-interlaced
- Automatic Movie mode detection and scanning

Standard Definition Input

- ITU-R BT.656/601 Video Input
- Separate H/V inputs synchronous with input clock
- 3D Temporal Noise Reduction with Comet-effect Correction
- Movie Mode Detection with Motion Phase Recovery
- Scene-change Detector for Contrast Enhancer and Up-conversion Control
- Letterbox Format Detection and Auto-Format Correction

High-Quality Video Display

- Picture Structure Improvement including Color Transition Improvement, Luma Peaking/Coring and Luma Contrast Enhancer
- H/V format conversion with Zoom In/Out (4x to 1/8x) with H/V decimation
- Letterbox and 4:3 to 16:9 format conversion with programmable 5-segment Panoramic mode
- Very flexible Sync Generator for Master and Slave modes by Vsync and Hsync signals with Line-locked Pixel Clock
- Progressive Display mode (60 Hz, 525 lines) for full-screen graphic planes
- Support for Monitor mode (VGA, SVGA and XGA)
- Mosaic mode with up to 16 pictures displayed

High-Performance 8-bit Bitmap OSD Generator

- Pixel-based resolution with 10-bit RGB outputs
- Programmable Resolution up to 1920x1024, all standard displays are supported:
  - Teletext 1.5 (480x520) and 2.5 (672x520)
  - Double-page Teletext (960x520) with Picture-and-Text
  - TeleWeb (640x480)
- 4 graphic planes with full alpha-blending capabilities:
  - 24-bit Background Plane
  - 10-bit RGB Video Plane
  - Bitmap OSD Plane with Color Map
  - Up to 128 x 128 pixel Cursor Plane
- 2D Graphics Accelerator

Embedded 32-bit ST20 CPU Core

Peripherals and I/Os for TV Chassis Control:

- 30 fully-programmable I/Os (5V tolerant)
- 4 external interrupts
- 8-bit programmable PWM with 4 inputs/outputs
- Infrared Digital Preprocessor
- Real Time Clock and Watchdog Timer
- 4 16-bit standard timers
- 10-bit ADC with 6 inputs and wake-up capability
- 2 Master/Slave I²C Bus Interfaces
- UART and support for IrDA interfaces

Teletext 1.5 and 2.5, Closed-Caption, VPS and WSS VBI Data Decoding, TeleWeb Compliant

Embedded Emulation Resources with In-Situ Flash Programming Capabilities

1.8V and 3.3V Power supplies

Eco Standby mode

27-MHz Crystal Oscillator

1 General Information

1.1 Introduction

This integrated circuit (IC) is dedicated to low-cost 100-Hz TV chassis. Combined with a digital multi-standard video decoder (STV2310) delivering an ITU-R BT.601/656 video stream and a 2H video scan IC, it provides a cost-effective, high-performance solution for 2H applications. The STV3500 includes a field or line up-converter, a 32-bit ST20 CPU core with all peripherals required for controlling the TV chassis. Teletext data is extracted from the incoming stream and decoded by the CPU. An embedded On-Screen Display (OSD) generator delivers the text and graphics. The Video Display Pipeline performs feature box image processing such as picture improvement, horizontal and vertical rescaling and Temporal Noise Reduction.

The chip operates with a single external SDRAM that is used for the field-rate up-conversion and text and graphic generations.The external SDRAM can be configured as a single bank of 16/64/128 Mb (16-bit configuration) or a dual bank of 16 to 256 Mb (32-bit configuration). Application program codes are stored in an external Flash memory and executed from the SDRAM.

The STV3500 is designed using an 0.18 micron CMOS process and delivered in a 160-pin PQFP (0.65 mm pitch) package.

The ST3500 completes the Digital IC Core family (STi5xxx, STi7xxx) which offers common CPU and software platforms based on STMicroelectronics' 32-bit ST20 CPU core.

Figure 1: Top Level Diagram

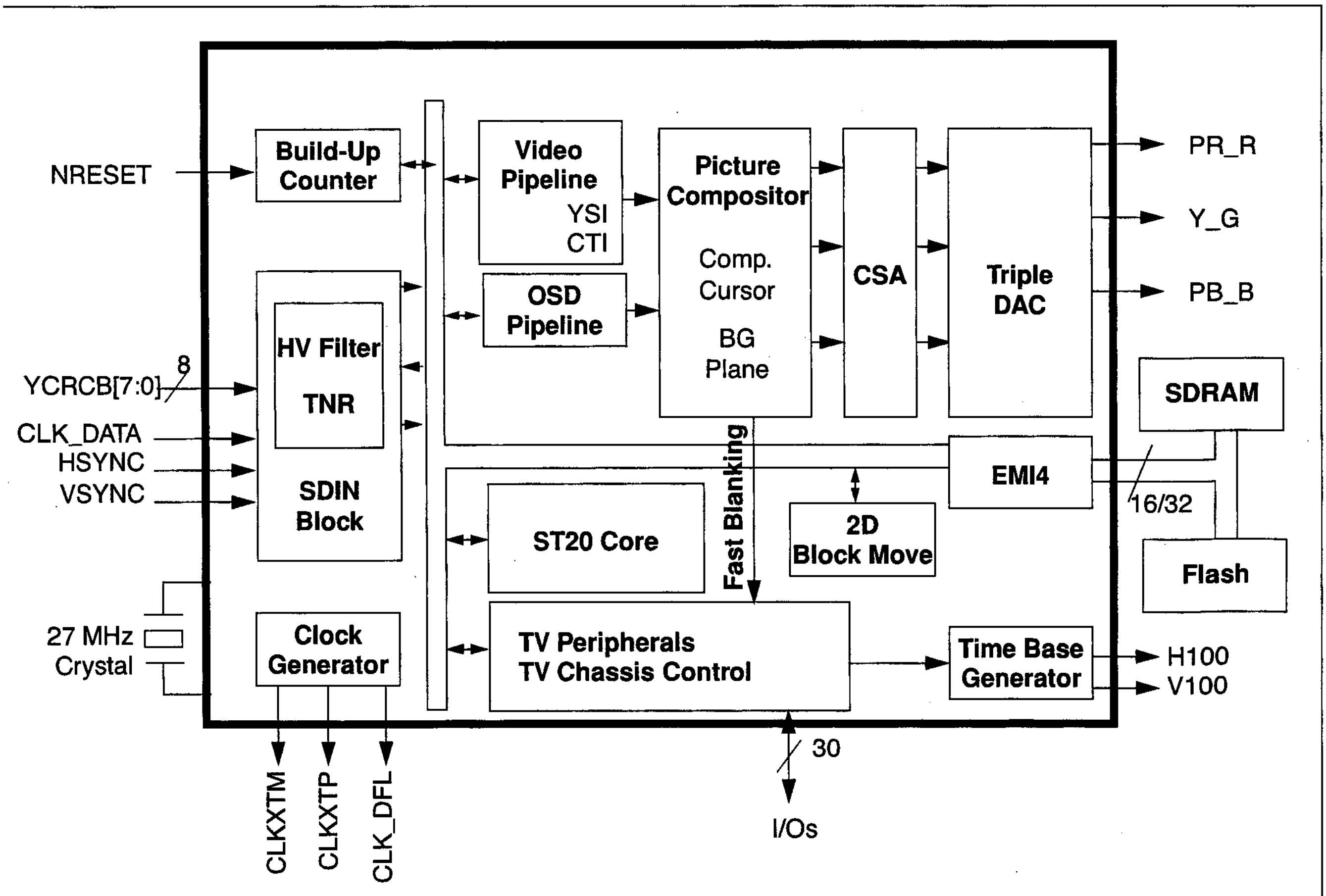
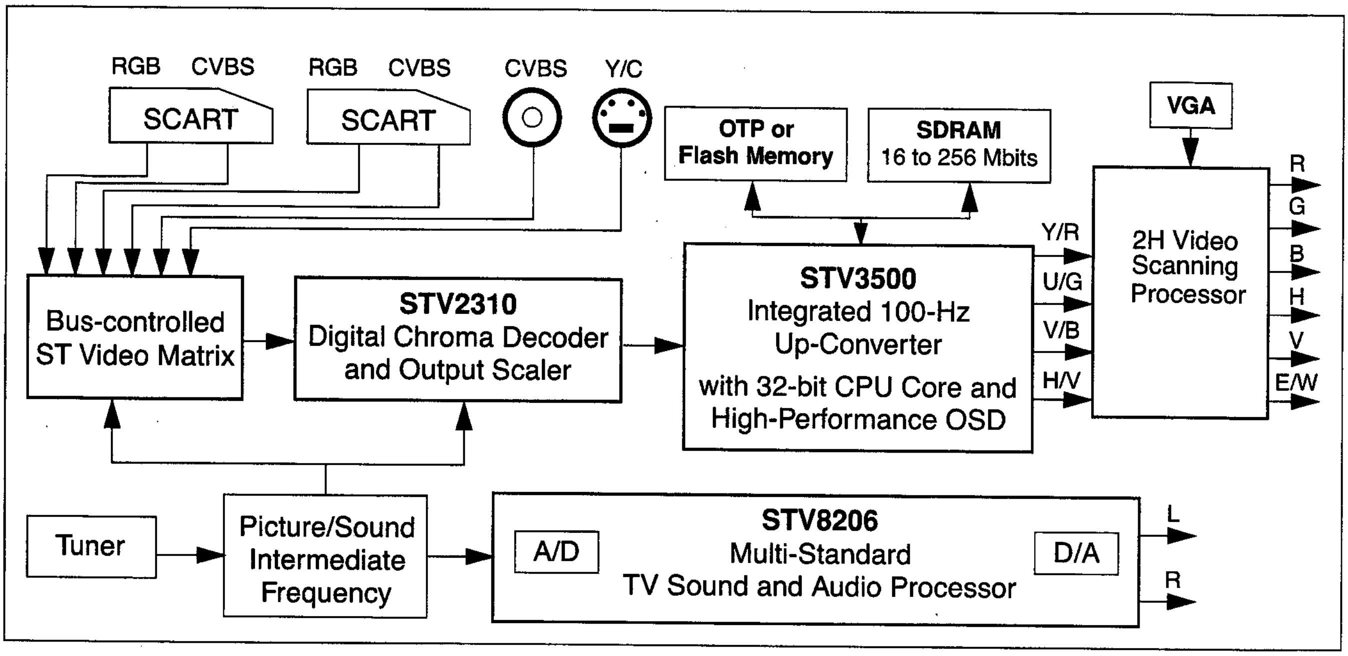


Figure 2: CTV100 Platform Diagram Example

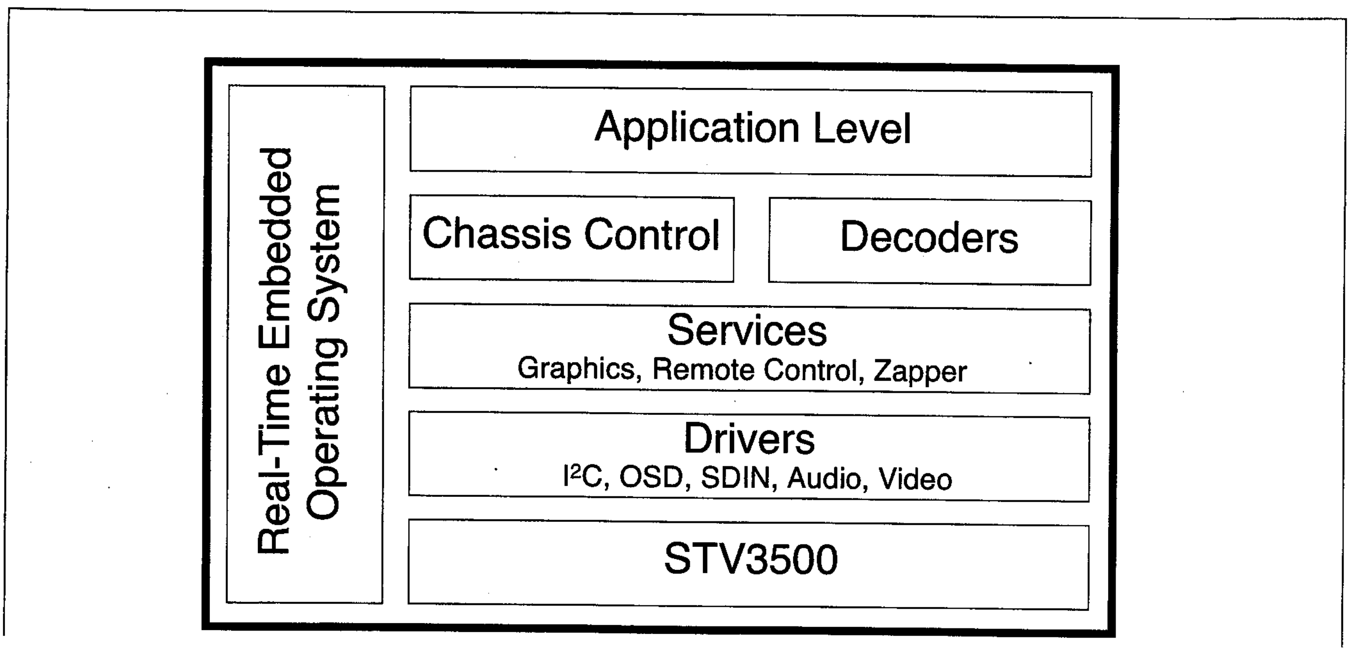


1.2 Software

The layering model adopted for the CTV100 Software Stack is based on certain non-functional requirements:

- Re-usable
- Portable
- Modular
- Reliable and robust
- Readable and maintainable

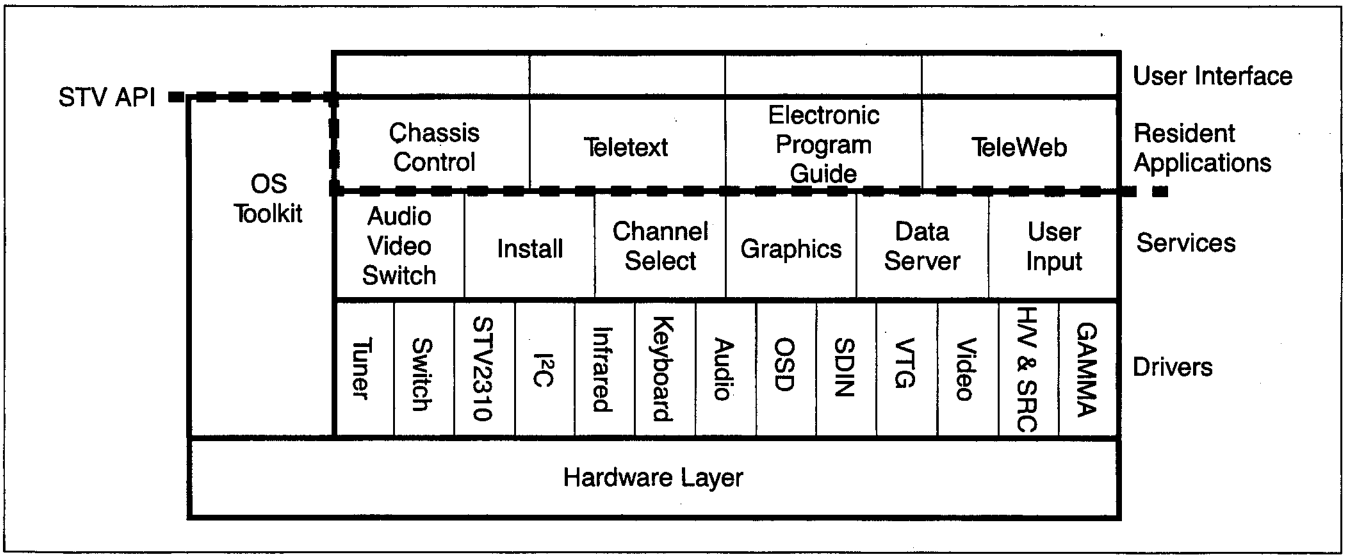
Figure 3: Global Software Architecture



The CTV100 application software consists of 4 main layers based on these non-functional requirements:

- System Layer provides certain general-purpose components such as Handle or Link List Managers. This layer also contains the Operating System Abstraction Layer (OSAL) components which enable other layers to be OS-independent.
- Driver Layer provides a hardware abstraction to the upper layers making them hardware-independent.
- Service Layer contains the components that provide the Application layer with high level interfaces in order to manage the TV set. The set of Service components included in the demonstration application are very useful for developing applications.
- Application Layer which contains the software that defines the “Look & Feel” of the TV set. This layer, for instance, contains the components that are responsible for the following features: interpretation of user inputs, display and navigation functions and Teletext applications.

Figure 4: Software Architecture Example



1.3 Related Documentation

There are several documents available that explain the various software capabilities. There are three different types of documents:

1. General Introduction Manual
2. User Guides
3. Reference Guide

1.3.1 General Introduction Manual

This document describes the general architecture of the features listed in Section 1.2: Software.

It also describes the relationships between the various service, driver, system and application modules. It lists all the available modules and their version number. A brief description of each function is also provided.

1.3.2 User Guides

A user guide is provided for each set of selected features. These documents will enable the user to get started with the relevant features. An example code is also included as well as a troubleshooting section.

A list (non-exhaustive) of existing user guides is given below.

1. CTV100: STV3500 User Controls User Guide
   - The Remote Control Service is responsible for the byte assembly of infrared frames coming from a Remote Control device. It provides the client with a high-level interface to manage Remote Control inputs.
   - The User Interface Service provides the client with a high-level interface to manage both Remote Control and Keyboard inputs. The client provides its own code, with which it will be notified.
2. CTV100: STV3500 Video and Sync User Guide
   - The Video Service provides the client with a high-level interface for managing the Video.

     This service is responsible for the complete management of the video buffers and the video display, according to client configuration, in terms of the video mode (Up-conversion, Proscan...).

     It also offers video-related features, such as zoom or freeze frame, among others.
   - The Synchronization Service is responsible for programming the field polarity. It provides the client with a high level interface for managing the Field Polarity sequences.
3. CTV100: STV3500 Source Selection User Guide
   - The Audio/Video Switch service is responsible for managing the connections between audio and video inputs and outputs by using drivers that provide audio/video switching functions.

     The Audio/Video Switch component is also responsible for detecting changes in the Slow Blanking Level (available on SCART connections) by using the ADC driver.
   - The Front End service is responsible for the tuning and the scanning operations. It provides the client with a high level interface working in the frequency domain.
4. CTV100: STV3500 Graphics User Guide
   - It provides the necessary software for creating cursors and graphic planes using respectively the Cursor Driver (DV_GAM) and the On-Screen Display Driver (STOSD).
   - It also includes the Two Dimensional Block Move Driver (DV_BME) in order to improve graphical applications which often require moving blocks of data.

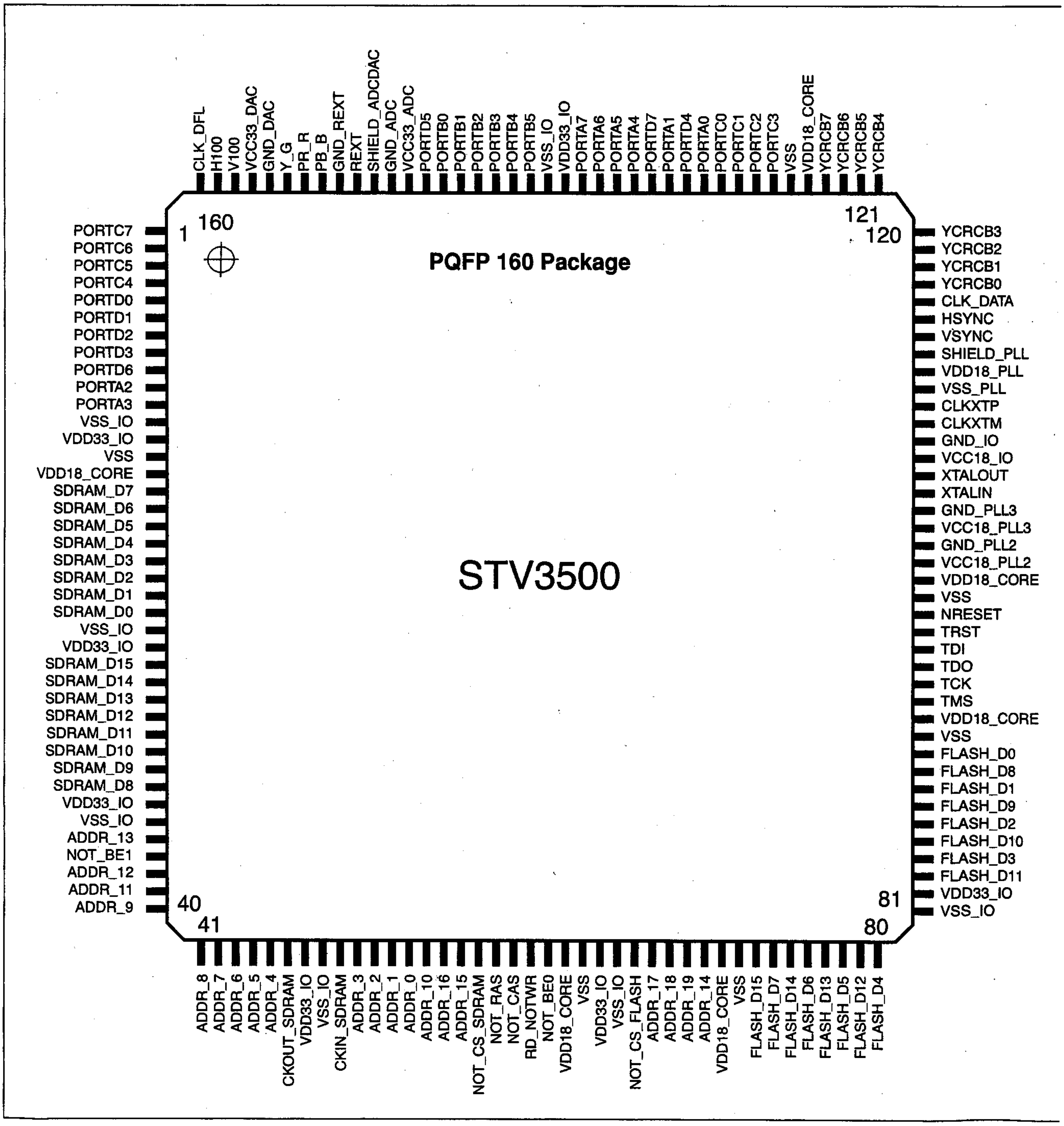
     This document will describe the CTV100 Basic Graphics Stack and also provide a guide for the implementation and configuration of a graphical user interface (GUI) stack based on the OSD.

1.3.3 Reference Guide

There is one reference guide for each component (service, driver, etc.). This document includes the API as well as an Example of Use. This document specifically targets design engineers.

2 STV3500 Pin List

2.1 Pinout Diagram



2.2 Pin Description

Table 1: Digital Video Input Stage

Pin No.	Pin Name	Pin Description	POR Value	If not used
114	VSYNC	Vertical Sync Input	Input	VSS_IO
115	HSYNC	Horizontal Sync Input	Input	VSS_IO
116	CLK_DATA	Video Input Clock from STV2310	Input	VSS_IO
117	YCRCB0	4:2:2 Data Stream Input 0 from STV2310	Input	VSS_IO
118	YCRCB1	4:2:2 Data Stream Input 1 from STV2310	Input	VSS_IO
119	YCRCB2	4:2:2 Data Stream Input 2 from STV2310	Input	VSS_IO
120	YCRCB3	4:2:2 Data Stream Input 3 from STV2310	Input	VSS_IO
121	YCRCB4	4:2:2 Data Stream Input 4 from STV2310	Input	VSS_IO
122	YCRCB5	4:2:2 Data Stream Input 5 from STV2310	Input	VSS_IO
123	YCRCB6	4:2:2 Data Stream Input 6 from STV2310	Input	VSS_IO
124	YCRCB7	4:2:2 Data Stream Input 7 from STV2310	Input	VSS_IO

Table 2: Video Output Stage

Pin No.	Pin Name	Pin Description	POR Value	If not used
Digital				
158	V100	Vertical Sync Output	3.3V	NC
159	H100	Horizontal Sync Output	3.3V	NC
160	CLK_DFL	Clock Output for Video/Scan Processor	0V	NC
Analog				
150	SHIELD_ADCDAC	To connect to ADC/DAC Analog Ground	0V	NC
151	REXT	External Reference Resistor for the Triple DAC	1.25V (Note 1)	NC
152	GND_REXT	Current Return for REXT	0V (Note 1)	NC
153	PB_B	Analog Pb/B Output	0.6V (Note 1)	NC
154	PR_R	Analog Pr/R Output	0.6V (Note 1)	NC
155	Y_G	Analog Y/G Output	0.6V (Note 1)	NC

Note: 1 Application dependent.

Table 3: Parallel Input/Output Pins (page 1 of 3)

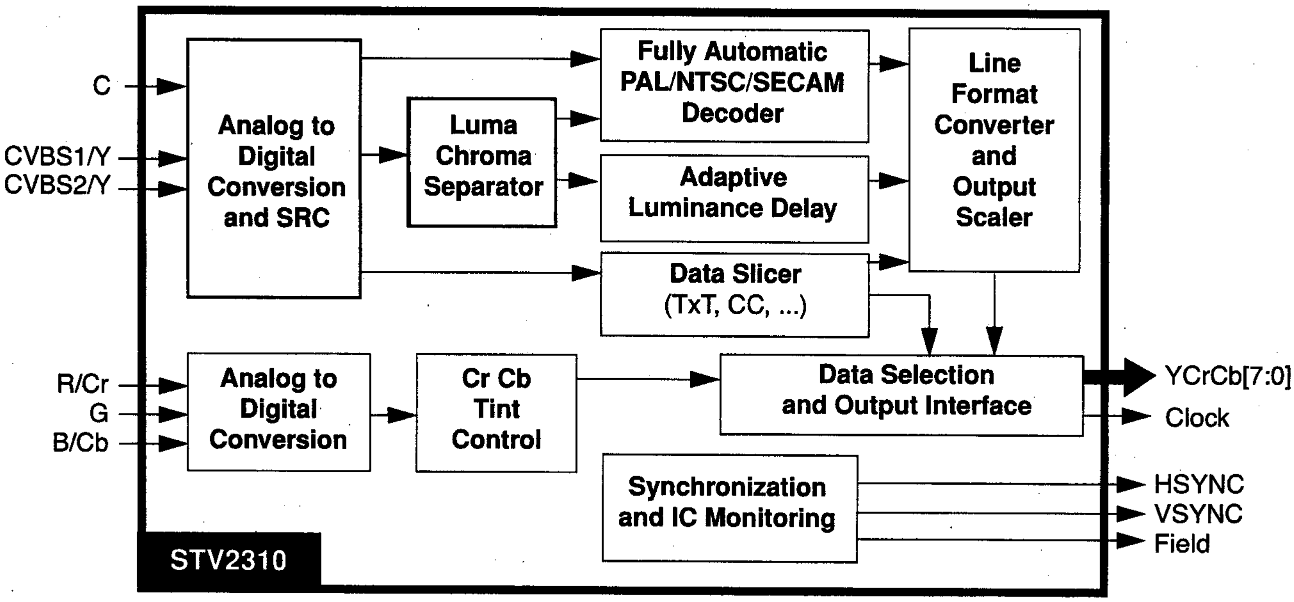
Pin No.	Pin Name	Main Function (after Reset)	Alternate Function	POR Value	If not used
131	PORTA0	Port A0	PWMCapture0/PWM0	Input	Output PP = 0, NC
133	PORTA1	Port A1	PWMCapture1/INT2/PWM1	Input	Output PP = 0, NC

Table 3: Parallel Input/Output Pins (page 2 of 3)

Pin No.	Pin Name	Main Function (after Reset)	Alternate Function	POR Value	If not used
10	PORTA2	Port A2	PWMCapture2/INT3/extrig/PWM2	Input	Output PP = 0, NC
11	PORTA3	Port A3	PWMCapture3/PWM3	Input	Output PP = 0, NC
135	PORTA4	Port A4	UARTF TXD	Input	Output PP = 0, NC
136	PORTA5	Port A5	UARTF RXD/UARTF TXD Smartcard	Input	Output PP = 0, NC
137	PORTA6	Port A6	UARTF CTS	Input	Output PP = 0, NC
138	PORTA7	Port A7	UARTF RTS	Input	Output PP = 0, NC
146	PORTB0	Port B0	AD_0	Input	Output PP = 0, NC
145	PORTB1	Port B1	AD_1	Input	Output PP = 0, NC
144	PORTB2	Port B2	AD_2	Input	Output PP = 0, NC
143	PORTB3	Port B3	AD_3	Input	Output PP = 0, NC
142	PORTB4	Port B4	AD_4 / Timer Output 0	Input	Output PP = 0, NC
141	PORTB5	Port B5	AD_5/ Timer Output 1	Input	Output PP = 0, NC
130	PORTC0	Port C0	SDA_0	Input	Output PP = 0, NC
129	PORTC1	Port C1	SCL_0	Input	Output PP = 0, NC
128	PORTC2	Port C2	SDA_1	Input	Output PP = 0, NC
127	PORTC3	Port C3	SCL_1	Input	Output PP = 0, NC
4	PORTC4	Port C4	SDA_2	Input	Output PP = 0, NC
3	PORTC5	Port C5	SCL_2	Input	Output PP = 0, NC
2	PORTC6	Port C6	SDA_3	Input	Output PP = 0, NC
1	PORTC7	Port C7	SCL_3	Input	Output PP = 0, NC
5	PORTD0	Port D0	Timer Input 0/CLK4OUT	Input	Output PP = 0, NC
6	PORTD1	Port D1	Timer Input 1/Hsync Input	Input	Output PP = 0, NC

STV2310

Multisandart TV/VCR Digital Video Decoder and Output Scaler



MAIN FEATURES

- Automatic NTSC/PAL/SECAM Digital Chroma Decoder
- Worldwide TV Standards Compatible
- VBI Data Slicer for Teletext, Closed Caption, WSS and other systems
- NTSC/PAL Adaptive 4H/2D Comb Filter
- Analog RGB/Fast Blanking Capture and Insertion in YCrCb Output Flow (SCART legacy)
- Analog YCrCb inputs with Tint Control
- Automatic Flesh Control on 117° or 123° Color Axis References
- NTSC Hue Control
- Line-locked ITU-R BT. 656/601 or Square Pixel YCrCb Outputs (Data and Clock)
- Orthogonal Correction on Output Pixels
- ITU-R BT.601 (and Square Pixel) Resolution for all Standards
- 8-bit Pixel Output Interface
- Programmable Horizontal Scaling (x0.25 to x4 Scaling Factor) and Panorama Vision
- Copy-Protection System compatible
- H and V Synchronization Processing that is robust to non-standard sources
- Single System Clock for all Video Input Formats
- Two-wire I C Bus Interface up to 400 kHz
- Typical Power Consumption: 500 mW
- Power Supply: 1.8 V and 3.3 V

The STV2310 is a high-quality front-end video circuit for processing all analog NTSC/PAL/SECAM standards into a 4:2:2 YCrCb video format. The STV2310 is programmable through an I2C interface.

The STV2310 provides a cost-effective solution for TV sets, STBs, DVD Recordable devices and PVR applications. It can be used as a stand-alone chip working with third-party products or as a companion chip to the STV3500 for 100-Hz or Progressive Scan TV sets.

1 General Description

The STV2310 is a high-quality video front-end circuit for processing all analog standards into a digitalized 4:2:2 YCrCb video format. It processes NTSC/PAL/SECAM CVBS signals, as well as conventional analog RGB or YCrCb signals.

This circuit outputs demodulated chrominance, in-phased luminance and sliced data for the most common services such as Teletext, Closed Caption, WSS, etc.

The STV2310 does not need an external synchronization system. It extracts all necessary synchronization signals from CVBS or Y signals, and delivers the horizontal, vertical and frame signals either on dedicated pins or embedded into the digital bit stream.

It features automatic standard recognition and automatic selection of the optimal Y/C separation algorithm according to the standard and has extensive output scaling capabilities. The STV2310 chip includes an analog RGB capture feature and programmable automatic mixing with the main picture digital output.

8-bit ITU-R BT.601/656 and Square Pixel output standards are supported.

The STV2310 provides a cost-effective solution for all applications where the analog TV signal is digitally processed: 100Hz/120Hz up-conversion, Digital Video Broadcast, High Definition Television, TV on PC, Set-Top Boxes, PVRs, etc.

All sub-level blocks operate at the frequency used as a sampling frequency (f_S) for the five embedded A/D converters. This free-running clock is called the system clock (f_S) and is provided either by an embedded crystal oscillator or an external clock generator (27 MHz).The only exception is the output stage which operates at the line-locked output pixel clock frequency.

Figure 1: Architectural Block Diagram

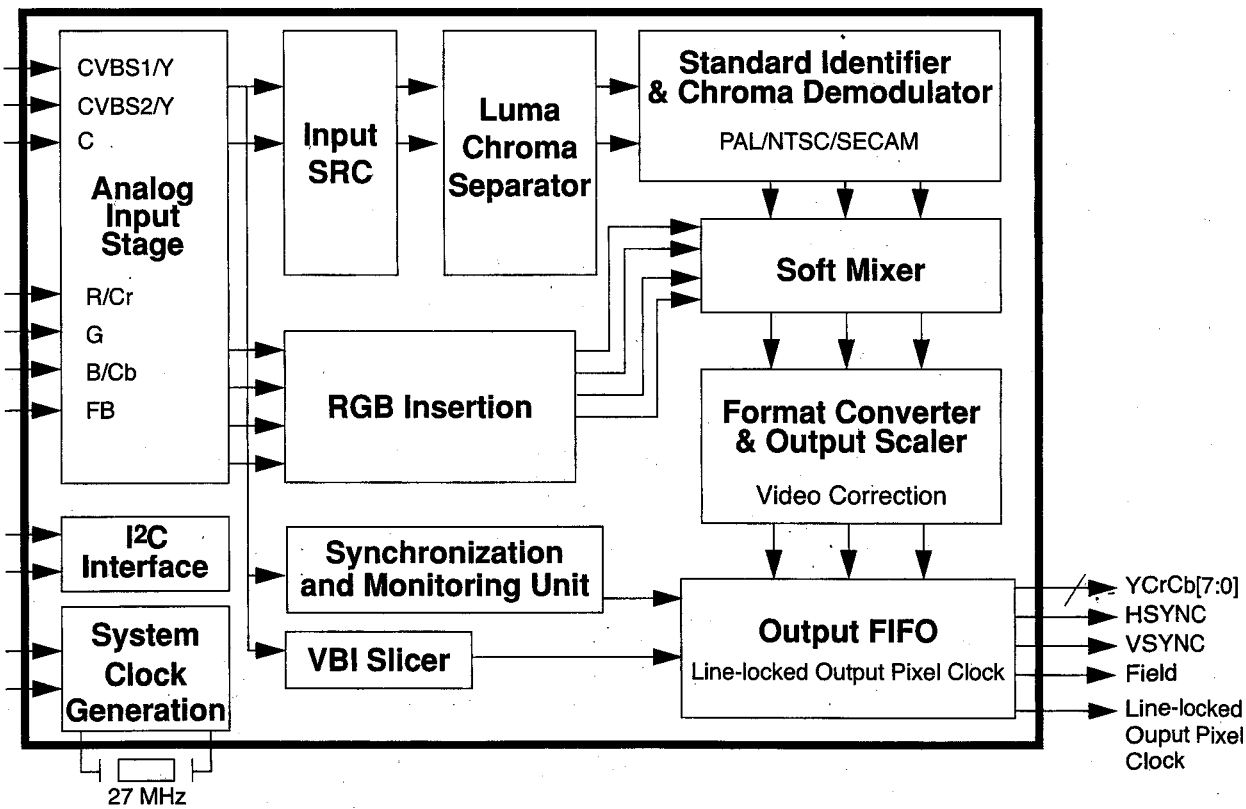
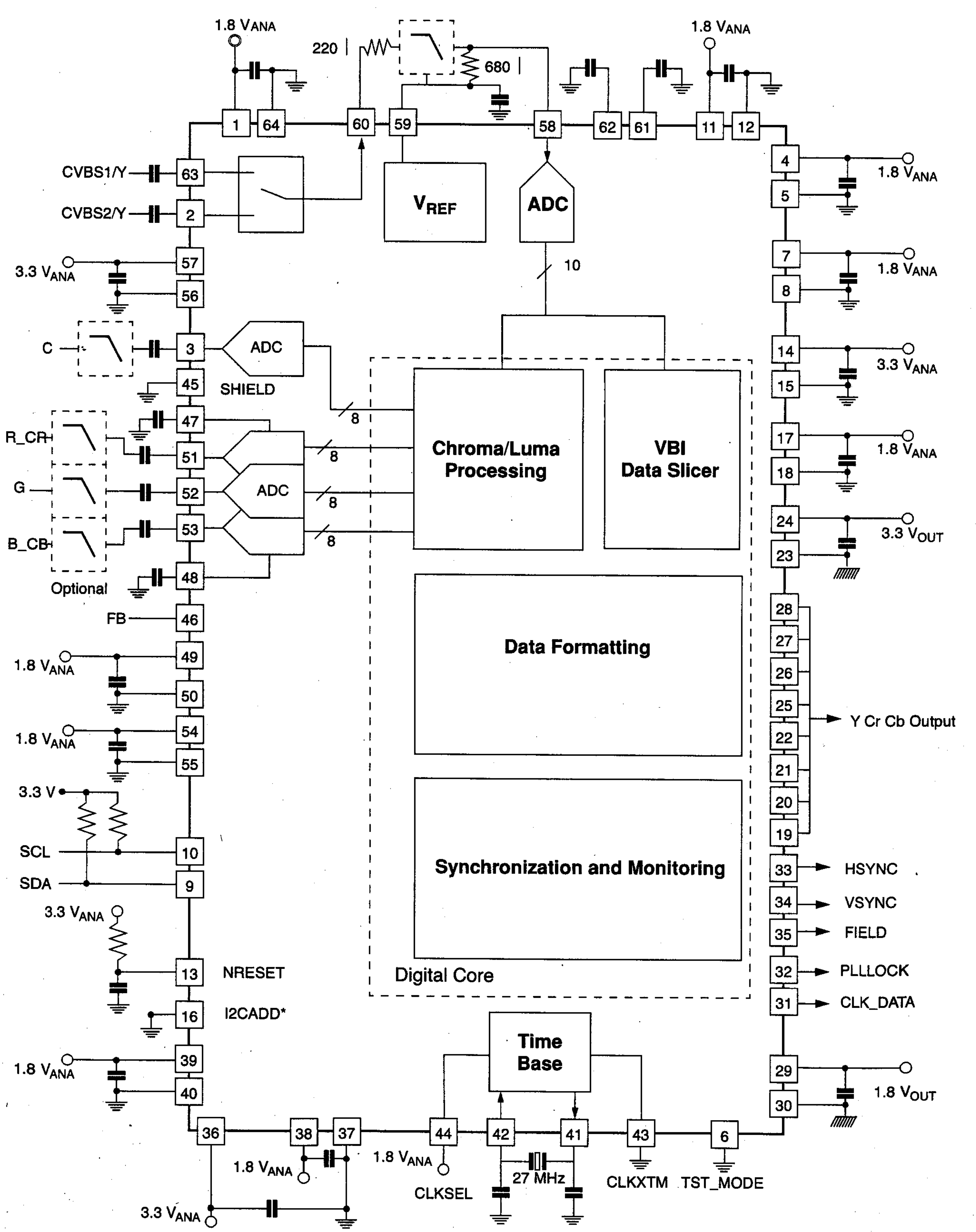


Figure 2: Application Block Diagram

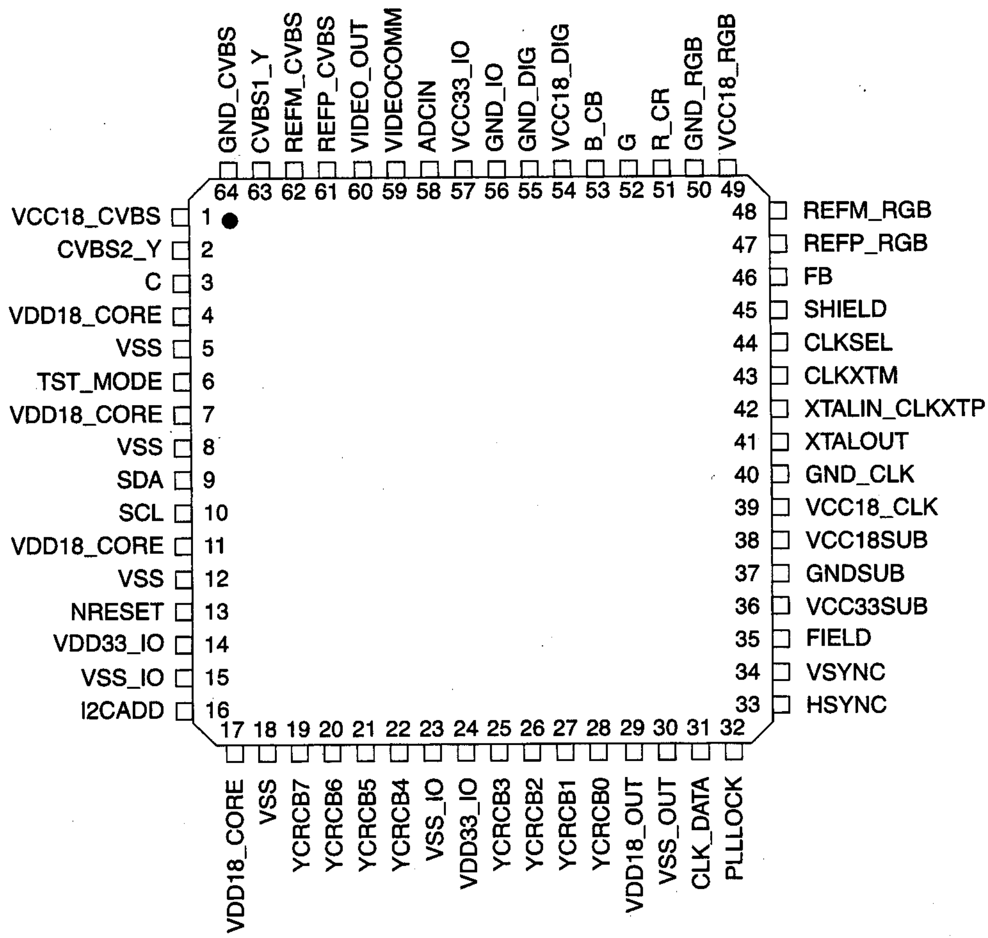


* Possible alternate I²C address. See **Section 5.1: Register Map on page 42**

2 Pin Allocation and Description

2.1 Pinout Diagram

Figure 3: 64-Pin 14 x 14 TQFP Package Pinout



2.2 Pin Descriptions

Table 1: Power Supply Pins (page 1 of 2)

Pin No.	Pin Name	Pin Description
Analog		
1	VCC18_CVBS	1.8 V Analog Voltage Supply for Analog Input Stage
36	VCC33SUB	3.3 V Analog Voltage Supply (Output and Pin Isolation layer)
37	GNDSUB	Analog Ground Supply (Substrate Polarization)
38	VCC18SUB	1.8 V Analog Voltage Supply (Output and Pin Isolation layer)

Table 1: Power Supply Pins (page 2 of 2)

Pin No.	Pin Name	Pin Description
39	VCC18_CLK	1.8 V Analog Voltage Supply for Clock Generator
40	GND_CLK	Analog Ground Supply for Clock Generator
45	SHIELD	Guard Ring (Analog Input Stage) To be connected to Analog Ground Supply
49	VCC18_RGB	1.8 V Analog Voltage Supply (RGB)
50	GND_RGB	Analog Ground Supply (RGB)
54	VCC18_DIG	1.8 V Analog Voltage Supply (Analog Input Stage)
55	GND_DIG	Analog Ground Supply (Analog Input Stage)
56	GND_IO	Analog Ground Supply (Analog Input Stage)
57	VCC33_IO	3.3 V Analog Voltage Supply (Analog Input Stage)
64	GND_CVBS	Analog Ground Supply (Analog Input Stage)
Digital		
4	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
5	VSS	Digital Ground Supply (Digital Core)
7	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
8	VSS	Digital Ground Supply (Digital Core)
11	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
12	VSS	Digital Ground Supply (Digital Core)
14	VDD33_IO	3.3 V Digital Voltage Supply for Pins (Digital Core)
15	VSS_IO	Digital Ground Supply for Pins
17	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
18	VSS	Digital Ground Supply (Digital Core)
23	VSS_IO	Digital Ground Supply for Pins and Outputs (Output Stage)
24	VDD33_IO	3.3 V Digital Voltage Supply for Pins (Output Stage)
29	VDD18_OUT	1.8 V Digital Voltage Supply (Output Stage)
30	VSS_OUT	Digital Ground Supply for Pins and Outputs (Output Stage)

Table 2: Analog Pins (page 1 of 2)

Pin No.	Pin Name	Pin Description
2	CVBS2_Y	CVBS or Y Input 2 (Selected by programming)
3	C	Chroma Input (Y/C inputs used for S-Video) (Selected by programming)
46	FB	Fast Blanking Input (To be used only when R_CR, G, and B_CB inputs are connected)
47	REFP_RGB	Positive Reference Voltage for RGB ADCs
48	REFM_RGB	Negative Reference Voltage for RGB ADCs

Table 2: Analog Pins (page 2 of 2)

Pin No.	Pin Name	Pin Description
51	R_CR	R Input for RGB Insertion. Cr Input for Analog YCrCb mode.
52	G	G Input for RGB Insertion.
53	B_CB	B Input for RGB Insertion. Cb Input for Analog YCrCb mode.
58	ADCIN	CVBS ADC Input (To be connected to Anti-Aliasing Filter output)
59	VIDEOCOMM	CVBS Anti-Aliasing Filter Reference Voltage
60	VIDEO_OUT	Video Analog Front-end Multiplexer Output for external filtering
61	REFP_CVBS	Positive Reference Voltage for CVBS and Chroma ADCs
62	REFM_CVBS	Negative Reference Voltage for CVBS and Chroma ADCs
63	CVBS1_Y	CVBS or Y Input 1 (Selected by programming)

Table 3: Output Pins

Pin No.	Pin Name	Type	Pin Description
19	YCRCB7	O	Digital Video Output 7
20	YCRCB6	O	Digital Video Output 6
21	YCRCB5	O	Digital Video Output 5
22	YCRCB4	O	Digital Video Output 4
25	YCRCB3	O	Digital Video Output 3
26	YCRCB2	O	Digital Video Output 2
27	YCRCB1	O	Digital Video Output 1
28	YCRCB0	O	Digital Video Output 0
31	CLK_DATA	O	Output Pixel Clock[1]
32	PLLLOCK	O	Output PLL Lock Signal Alternate Function: PIO[0] Bus extension
33	HSYNC	O	Horizontal Synchronization Pulse Output Alternate Function: PIO[1] Bus extension
34	VSYNC	O	Vertical Synchronization Pulse Output Alternate Function: PIO[2] Bus extension
35	FIELD	O	Field (Parity) Output Signal Alternate Function: PIO[3] Bus extension

1. All other outputs are synchronous to the rising or falling edge of the output pixel clock according to programming.

Table 4: Clock Signal Pins

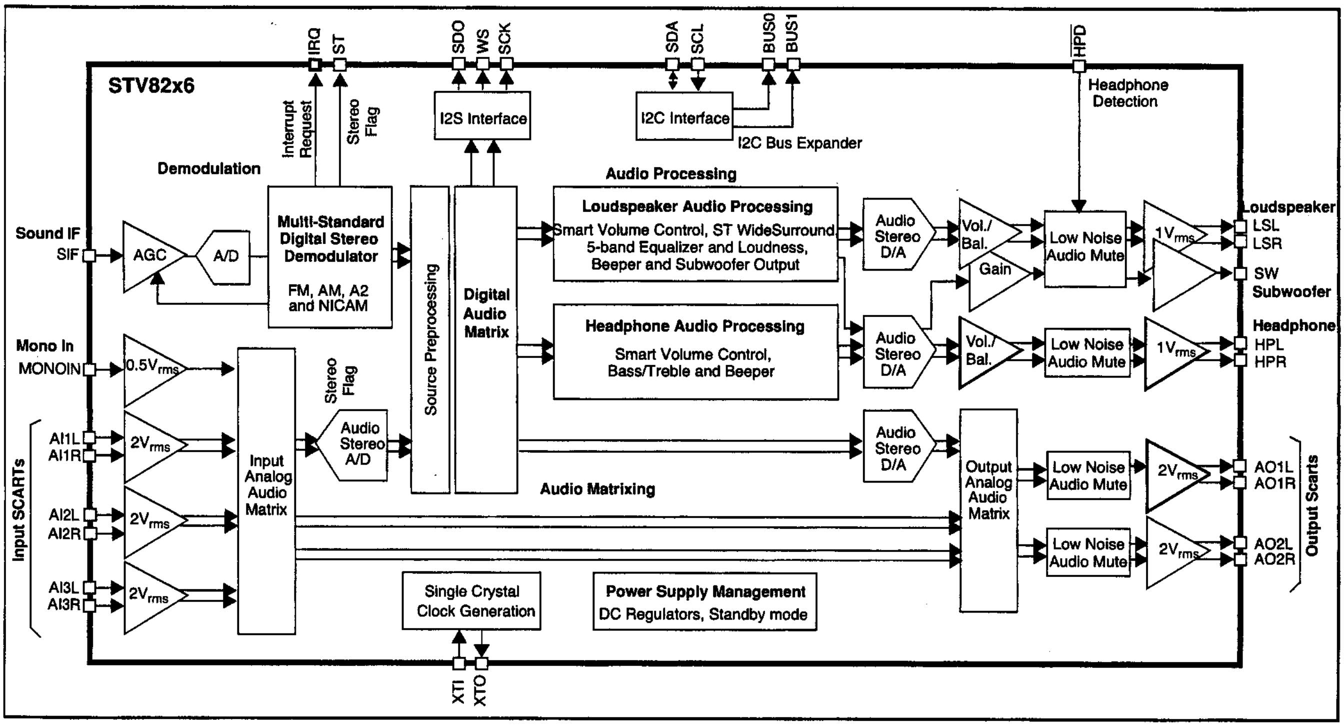
Pin No.	Pin Name	Pin Description
41	XTALOUT	Crystal Pad Oscillator Output
42	XTALIN_CLKXTP	Crystal Pad Oscillator Input Alternate Function: Differential Clock input
43	CLKXTM	Differential Clock input (To be used in conjunction with CLKXTP)

Table 5: Configuration Pins

Pin No.	Pin Name	Type	Pin Description
6	TST_MODE	I	Test Mode (Must be tied low in Normal mode)
9	SDA	I/O	I^2C Bus Data
10	SCL	I/O	I^2C Bus Clock
13	NRESET	I	Hardware Reset (Active low)
16	I2CADD	I	I^2C Address Selection (Must be tied high or low according to selected I^2C address). See **Section 5.1: Register Map on page 42** 0: 86h/87h 1: 8Eh/8Fh
44	CLKSEL	I	Input Clock Selection (Must be coherent with XTALIN_CLKXTP and CLKXTM connections) 0: CLKXTP and CLKXTM 1: XTAL

STV82x6

Multistandard TV Audio Processor and Digital Sound Demodulator



This device incorporates the SRS (Sound Retrieval System) under licence from SRS Labs, Inc.

Key Features

- NICAM, AM, FM Mono and FM 2 Carrier Stereo Demodulators for all sound carriers between 4.5 and 7 MHz
- Mono input provided for optimum AM Demodulation performances
- Demodulation controlled by Automatic Standard Recognition System
- Sound IF AGC with wide range
- Overmodulation and Carrier Offset recovery
- Smart Volume Control
- 5-band Equalizer & Bass/Treble Control
- Automatic Loudness Control
- Loudspeaker and Headphone outputs with Volume/Balance Controls and Beeper
- Subwoofer output with Volume Control and Programmable Bandwidth
- Spatial Sound Effects (ST WideSurround and Pseudo-Stereo)
- SRS® 3D Surround
- 3-to-2 Analog Stereo Audio I/Os (SCART compatible) with Audio Matrix
- Low-noise Audio Mutes and Switches
- I S Output to interface with Dolby® Pro Logic® Decoder
- I2C Bus-controlled
- Single and standard 27 MHz Crystal Oscillator
- Power supplies: 3.3 V Digital, 5 V or 8 V Analog
- Embedded 3.3 V Regulators
- Packages: SDIP56 or TQFP80

1 General Description

1.1 Overview

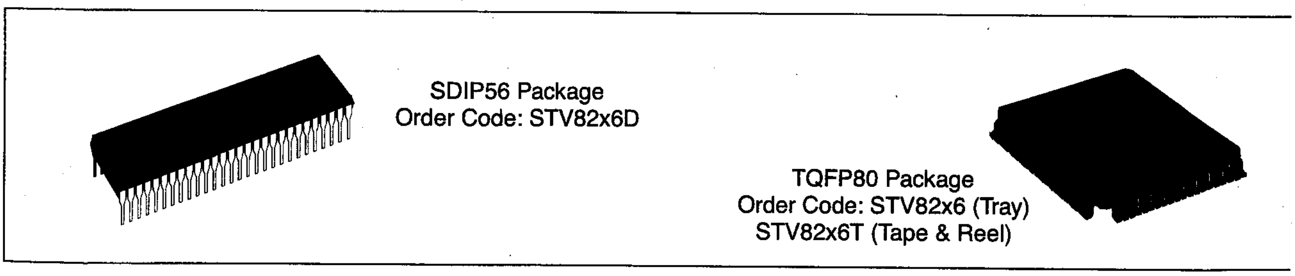
The STV82x6 is composed of three main parts:

1. **TV Sound Demodulator**: provides all the necessary circuitry for the demodulation of audi transmissions of European and Asian terrestrial TV broadcasts. The various transmission standards are automatically detected and demodulated without user intervention.
2. **Audio Processor**: based on DSP technology, independently controls loudspeaker, subwo and headphone signals. It offers basic and advanced features, such as a ST WideSurroun Equalizer, Automatic Loudness and Smart Volume Control for television viewer comfort. Tl STV8226/36 versions can perform additionally the SRS® 3D Surround for stereo and mor signals.
3. **Audio Matrix**: 3 stereo and 1 mono external analog audio inputs to loudspeakers and headphone, with 2 stereo external analog audio outputs (SCART compatible).

Table 1: STV82x6 Version List

Feature	STV8206	STV8216	STV8226	STV82:
AM-FM Mono	X	X	X	X
Zweiton	X	X	X	X
NICAM		X		X
ST WideSurround	X	X	X	X
SRS® 3D Surround			X	X

Figure 1: Package Ordering Information



1.2 Typical Applications

Figure 2: Typical Application (Low-cost Stereo TV)

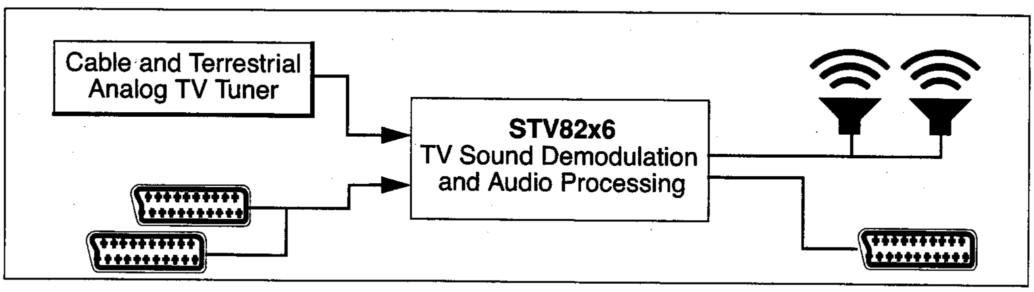


Figure 3: Typical Application with Sub-woofer and Headphone

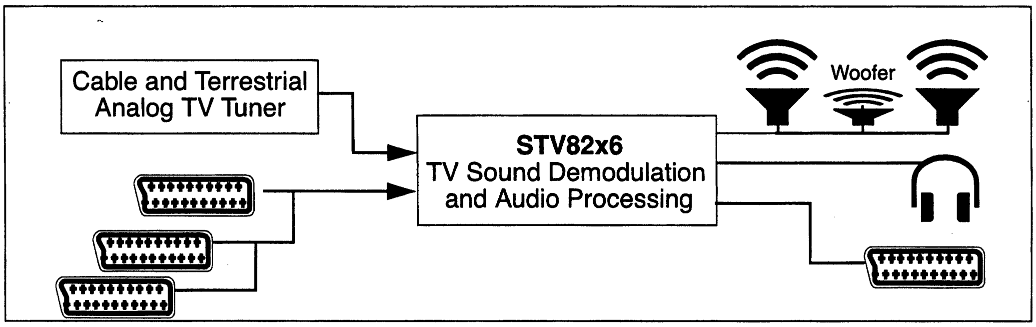


Figure 4: Typical Application Electrical Diagram for STV82x6 in SDIP56 package

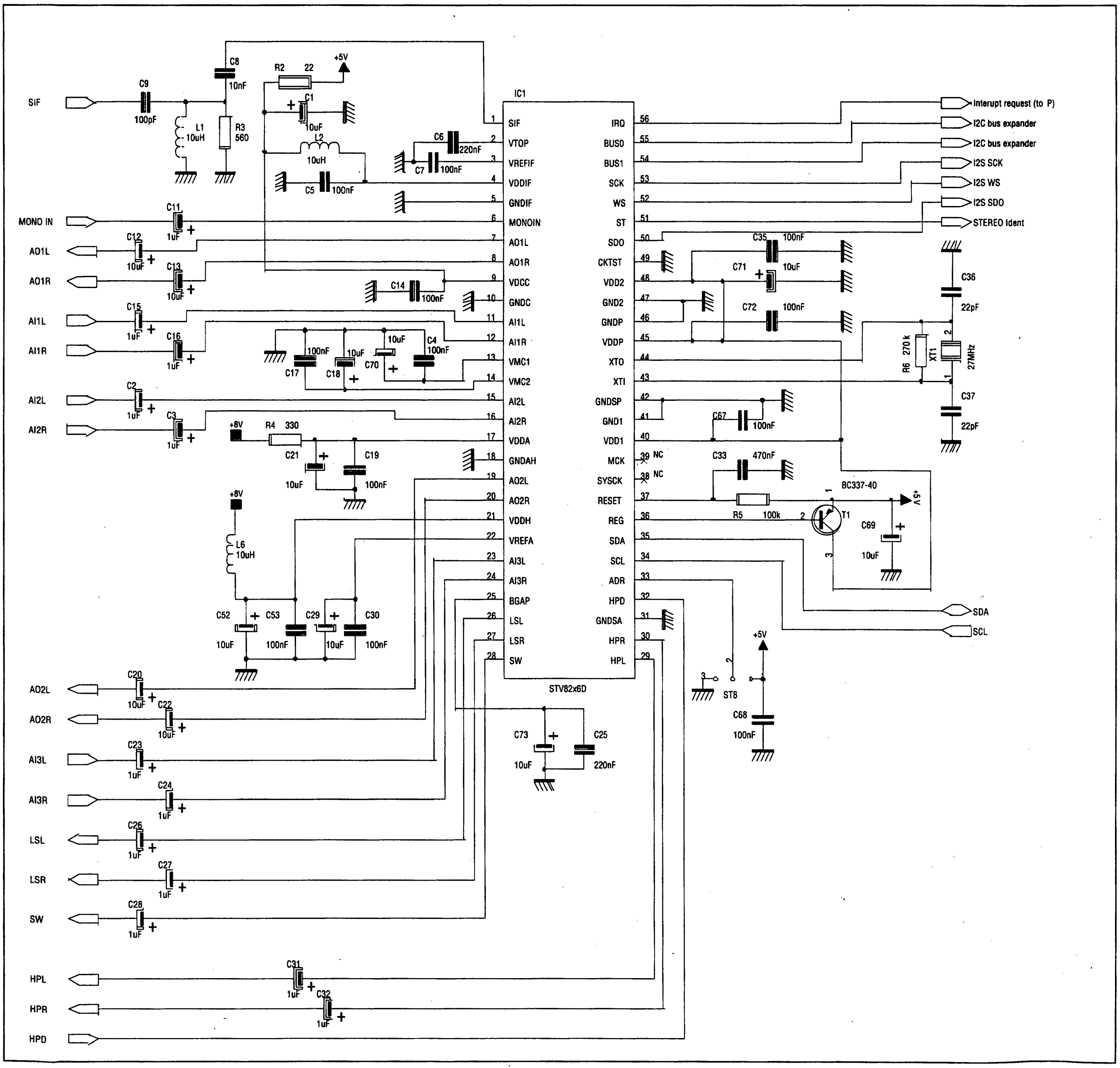
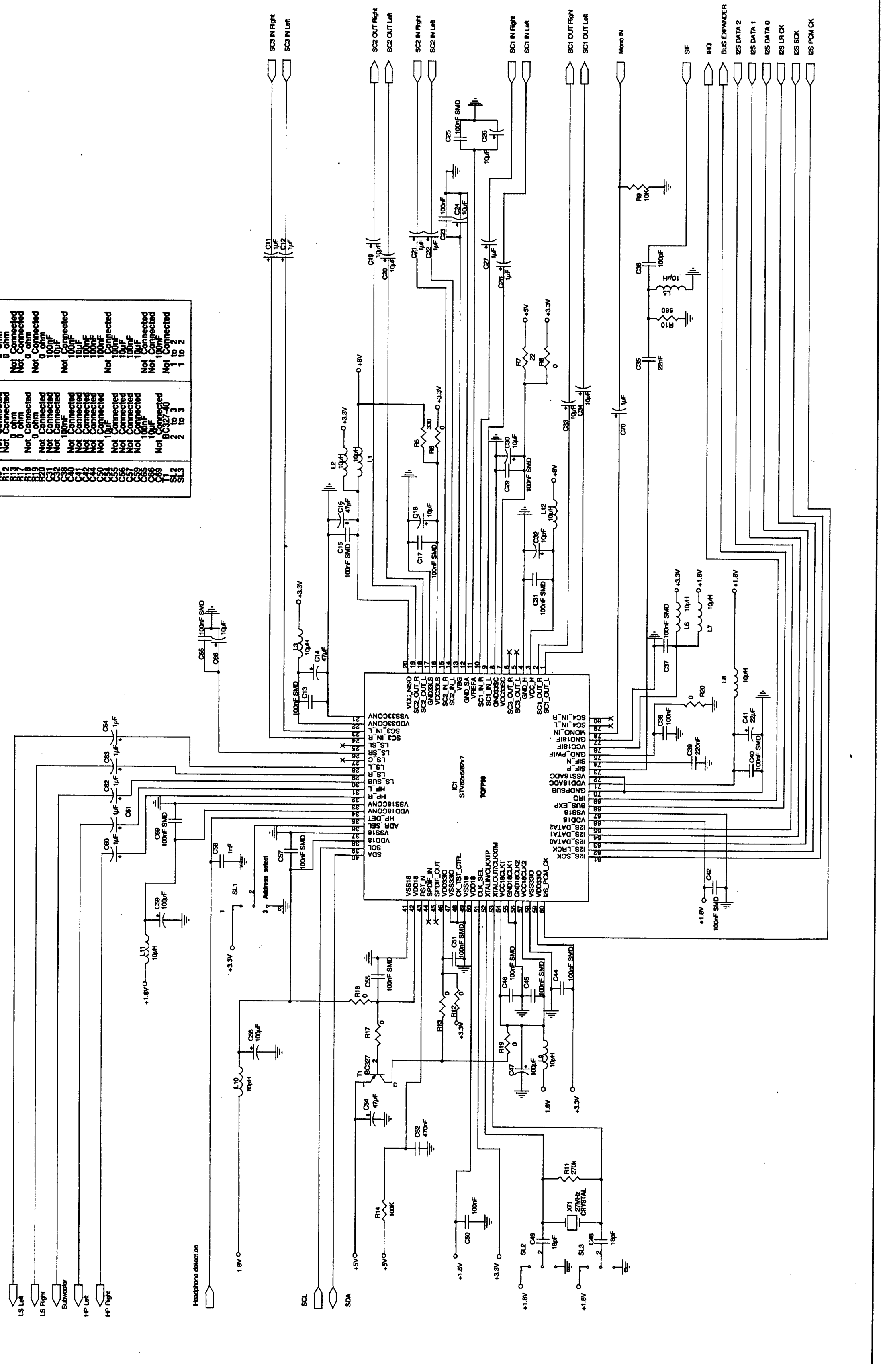


Figure 5: Typical Compatible Application Electrical Diagram for STV82x6 and STV82x7 in TQFP80 package



Part	with STV82x6	with STV82x7
L1	10µH	Not Connected
L2	Not Connected	10µH
L3	Not Connected	10µH
L6	10µH	Not Connected
L7	Not Connected	10µH
L8	Not Connected	10µH
L9	Not Connected	10µH
L10	Not Connected	10µH
L11	Not Connected	10µH
L12	Not Connected	10µH
R5	330 ohms	Not Connected
R6	Not Connected	0 ohm
R7	22 ohms	Not Connected
R8	Not Connected	0 ohm
R12	Not Connected	0 ohm
R13	0 ohm	Not Connected
R17	0 ohm	Not Connected
R18	Not Connected	0 ohm
R19	0 ohm	Not Connected
R20	Not Connected	0 ohm
C31	Not Connected	100nF
C32	Not Connected	10µF
C38	100nF	Not Connected
C40	Not Connected	100nF
C41	Not Connected	10µF
C42	Not Connected	100nF
C44	Not Connected	100nF
C50	Not Connected	100nF
C54	10µF	Not Connected
C55	Not Connected	100nF
C56	Not Connected	10µF
C57	Not Connected	100nF
C59	Not Connected	10µF
C65	100nF	Not Connected
C66	10µF	Not Connected
C69	Not Connected	100nF
T1	BC327-40	Not Connected
SL2	2 to 3	1 to 2
SL3	2 to 3	1 to 2

1.3 I/O Pin Description

Legend / Abbreviations for Table 2:

Type:

- AP = Analog Power Supply
- DP = Digital Power Supply
- I = Input
- O = Output
- OD = Open Drain
- B = Bidirectional
- A = Analog

Table 2: Pin Description

SDIP 56	TQFP 80	Name	Type	Function
1	73	SIF	A	Sound IF Input
2	74	VTOP	A	ADC V_{TOP} Decoupling Pin
3	75	VREFIF	A	AGC Voltage Reference Decoupling Pin
4	76	VDDIF	AP	3.3 V Power Supply for IF AGC & ADC
5	77	GNDIF	AP	0 V Power Supply for IF AGC & ADC
6	78	MONOIN	A	Mono Input
	79/80	N/C		Not Used
7	1	AO1L	A	Left SCART1 Audio Output
8	2	AO1R	A	Right SCART1 Audio Output
-	3/4/5/6	N/C		Not used
9	7	VDDC	AP	3.3 V Power Supply for Audio DAC/ADC
10	8	GNDC	AP	0 V Power Supply for DAC/ADC
11	9	AI1L	A	Left SCART1 Audio Input
12	10	AI1R	A	Right SCART1 Audio Input
13	11	VMC1	A	Switched V_{REF} Decoupling Pin for Audio Converters (VMCP)
14	13	VMC2	A	V_{REF} Decoupling Pin for Audio Converters (VMC)
15	14	AI2L	A	Left SCART2 Audio Input
16	15	AI2R	A	Right SCART2 Audio Input
17	16	VDDA	AP	3.3 V Power Supply for Audio Buffers, Matrix & Bias
18	17	GNDAH	AP	0 V Power Supply for Audio Buffers & SCART
19	18	AO2L	A	Left SCART2 Audio Output
20	19	AO2R	A	Right SCART2 Audio Output
21	20	VDDH	AP	8 V / 5 V Power Supply for SCART & Audio Buffers
-	21	N/C		Not Used
22	22	VREFA	A	Voltage Reference for Audio Buffers
23	23	AI3L	A	Left SCART3 Audio Input
24	24	AI3R	A	Right SCART3 Audio Input
-	25	N/C		Not Used
25	26	BGAP	A	Bandgap Voltage Source Decoupling
-	27	N/C		Not Used

Table 2: Pin Description (Continued)

SDIP 56	TQFP 80	Name	Type	Function
26	28	LSL	A	Left Loudspeaker Output
27	29	LSR	A	Right Loudspeaker Output
28	30	SW	A	Subwoofer Output
29	31	HPL	A	Left Headphone Output
30	32	HPR	A	Right Headphone Output
31	33	GNDSA	AP	Substrate Analog/Digital Shield
-	34	N/C		Not Used
32	35	$\overline{\text{HPD}}$	B	Headphone Detection Input (Active Low)
33	36	ADR	I	Hardware I²C Chip Address Control
-	37/38	N/C		Not Used
34	39	SCL	OD	I²C Serial Clock
35	40	SDA	OD	I²C Serial Data
-	41	N/C		Not Used
36	42	REG	A	5 V Power Regulator Control
37	43	$\overline{\text{RESET}}$	I	Hardware Reset (Active Low)
38	44	SYSCK	B	System Clock Output
39	45	MCK	B	I²S Master Clock Output
40	46	VDD1	DP	3.3V Power Supply for Digital Core & IO Cells
41	47	GND1	DP	0V Power Supply for Digital Core & IO Cells
-	48	N/C		Not Used
42	49	GNDSP	AP	Substrate Analog/Digital Shield for Clock-PLL
	50/51	N/C		Not Used
43	52	XTI	I	Crystal Oscillator Input
44	53	XTO	O	Crystal Oscillator Output
45	54	VDDP	AP	3.3 V Power Supply for Analog PLL Clock
46	55	GNDP	AP	0 V Power Supply for Analog PLL Clock
47	56	GND2	DP	0 V Power Supply for Digital Core, DSPs & IO Cells
48	57	VDD2	DP	3.3 V Power Supply for Digital Core, DSPs & IO Cells
49	58	CKTST	I	Must be Connected to 0 V
-	59/60	N/C		Not Used
50	61	SDO	B	I²S Bus Data Output
51	62	ST/SDI	B	Stereo Detection Output / I²S Bus Data Input
52	63	WS	B	I²S Bus Word Select Output
53	64	SCK	B	I²S Bus Clock Output
54	65	BUS1	B	I²C Bus Expander Output 1
-	66/67	N/C		Not Used
55	68	BUS0	B	I²C Bus Expander Output 2
56	69	IRQ	B	I²C Status Read Request
-	70	N/C		Not Used
-	71	N/C		Not Used
-	72	N/C		Not Used

STV9379A

Vertical Deflection Booster

FEATURES

- Power Amplifier
- Flyback Generator
- Thermal Protection
- Output Current up to 2.6 App
- Flyback Voltage up to 90V (on pin 5)
- Suitable for DC Coupling Application

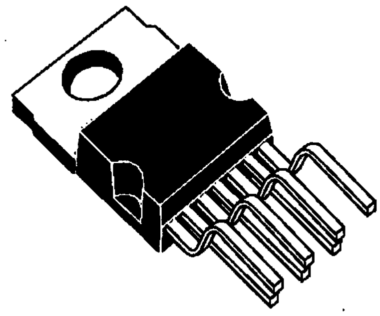
DESCRIPTION

Designed for monitors and high performance TVs, the STV9379A vertical deflection booster delivers flyback voltages close to 90V.

The STV9379A operates with supplies up to 42V and provides up to 2.6 A_{PP} output current to drive the yoke.

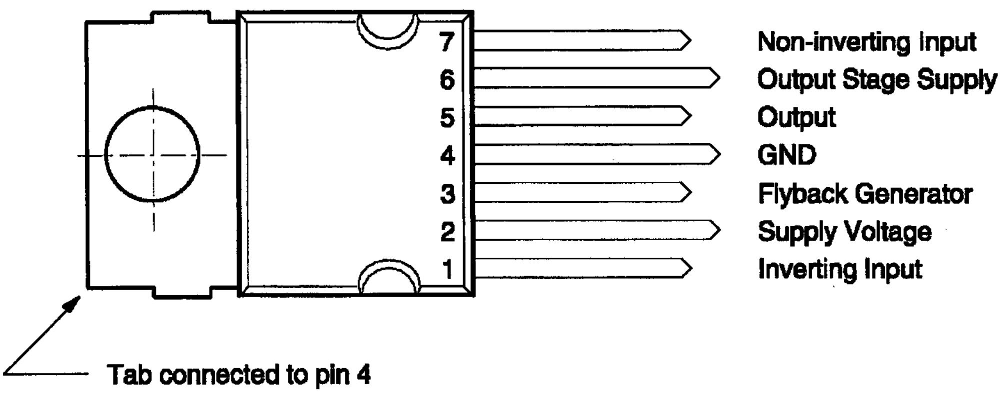
The STV9379A is inserted in HEPTAWATT package.

PACKAGE



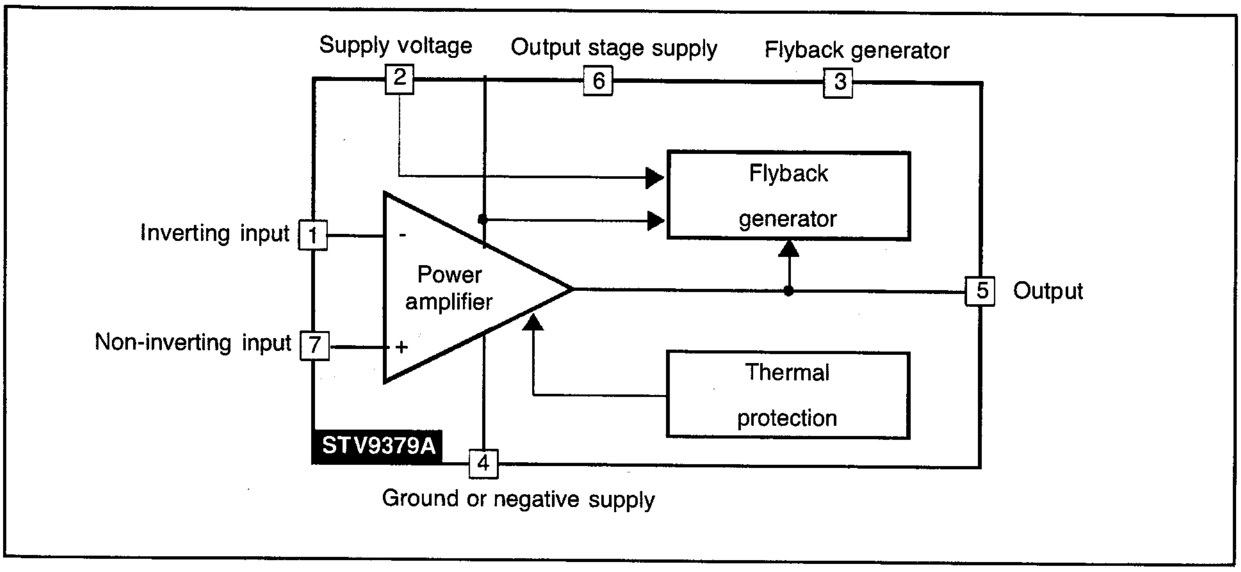
HEPTAWATT
(Plastic Package)
ORDER CODE: STV9379A

PIN CONNECTION



Block Diagram

Figure 1. STV9379A block diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pin 2) (Note 1)	50	V
V_6	Flyback Peak Voltage (Pin 6) (Note 1)	100	V
V_1,V_7	Amplifier Input Voltage (Pins 1-7) (Note 1)	-0.3, + V_S	V
I_O	Maximum Output Peak Current (Note 2, Note 3)	1.8	A
I_3	Maximum Sink Current (first part of flyback) (t < 1ms)	1.8	A
I_3	Maximum Source Current (t < 1ms) (Note 2)	1.8	A
V_{ESD}	ESD Susceptibility: EIAJ Norm (200pF discharged through 0Ω)	300	V
T_{oper}	Operating Ambient Temperature	-20, +75	ϒC
T_{stg}	Storage Temperature	-40, +150	ϒC
T_j	Junction Temperature	+ 150	ϒC

Note 1: Versus Pin 4.
Note 2: The output current can reach 5A peak for t ″ 10µs (up to 120Hz)
Note 3: Provided SOAR is respected (see Figures 1 and 2).

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-c)}$	Junction-Case Thermal Resistance Max.	3	ϒC/W
T_t	Temperature for Thermal Shutdown	150	ϒC
ΔT_t	Hysteresis on Tt	10	ϒC
T_{jr}	Recommended Max. Junction Temperature	120	ϒC

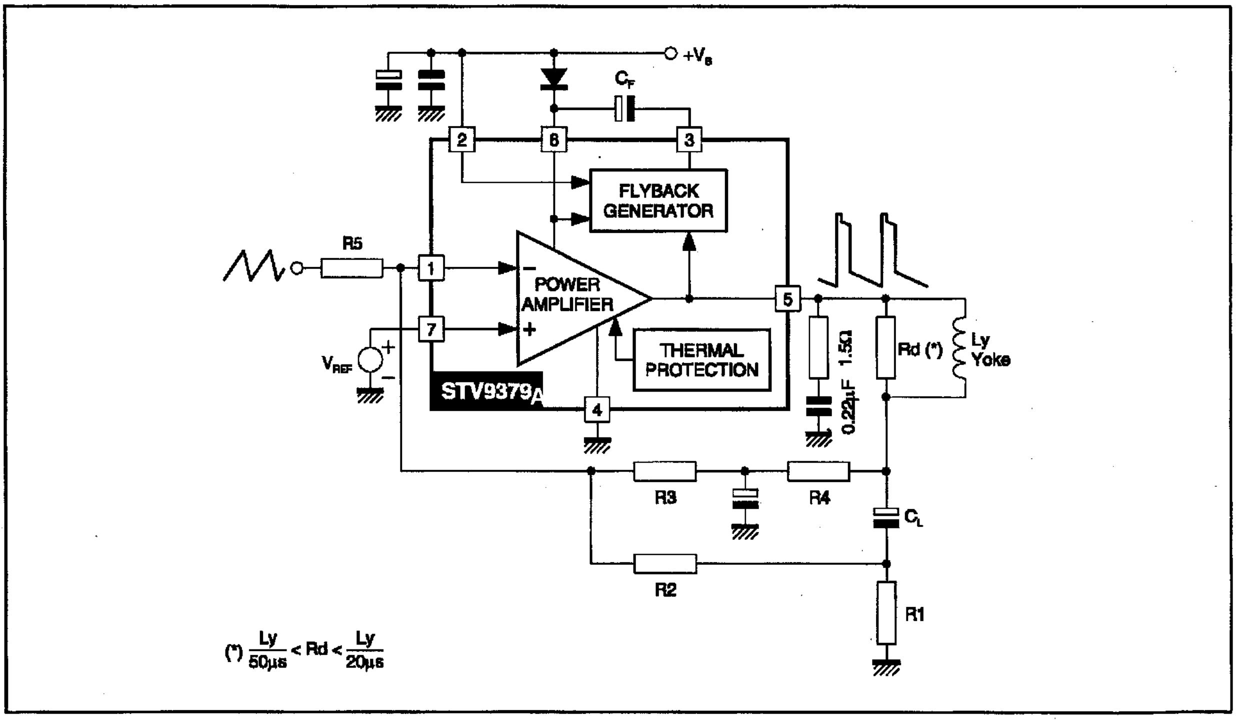
ELECTRICAL CHARACTERISTICS

V_S=42V, T_A = 25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range	Versus Pin 4	10		42	V
I_2	Pin 2 Quiescent Current	$I_3 = 0$, $I_5 = 0$		13	20	mA
I_6	Pin 6 Quiescent Current	$I_3 = 0$, $I_5 = 0$	5	10	30	mA
I_o	Max. Peak Output Current				1.3	A
I_1	Amplifier Bias Current	V_1 = 25V, V_7 = 26V		-0.15	- 1	µA
I_7	Amplifier Bias Current	V_1 = 26V, V_7 = 25V		-0.15	- 1	µA
V_{IO}	Offset Voltage				7	mV
$\Delta V_{IO}/dt$	Offset Drift Versus Temperature			- 10		µV/°C
GV	Voltage Gain		80			dB
V_{5L}	Output Saturation Voltage to GND (Pin 4)	I_5 = 1.3A		1	1.5	V
V_{5H}	Output Saturation Voltage to Supply (Pin 6)	I_5 = -1.3A		1.6	2.1	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	I_5 = 1.3A		1.3	2	V
V_{D3-2}	Diode Forward Voltage between Pins 3-2	I_3 = 1.3A		1.3	2	V
V_{3L}	Saturation Voltage on Pin 3	I_3 = 20mA		0.8	1.2	V
V_{3SH}	Saturation Voltage to Pin 2 (2nd part of flyback)	I_3 = - 1.3A		2.9	3.6	V

APPLICATION CIRCUITS

AC COUPLING



APPLICATION CIRCUITS (CONTINUED)

DC COUPLING.

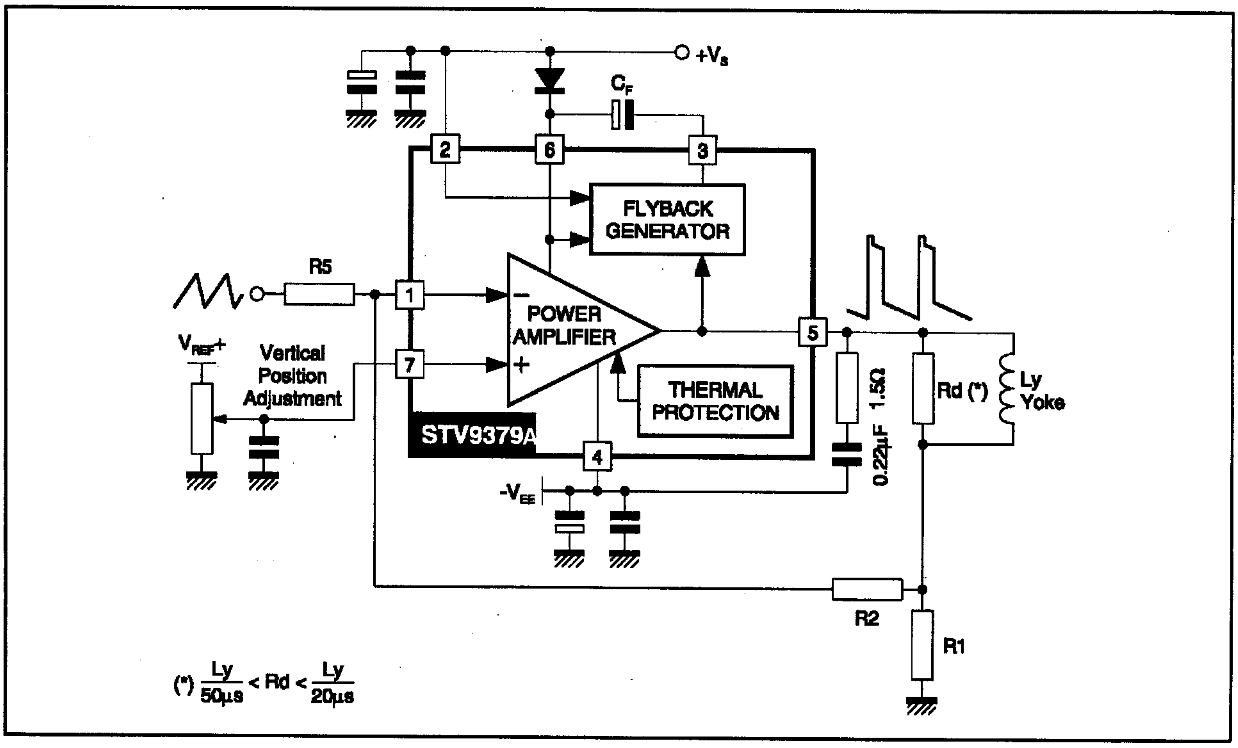


Figure 2. Output transistors SOA (for secondary breakdown)

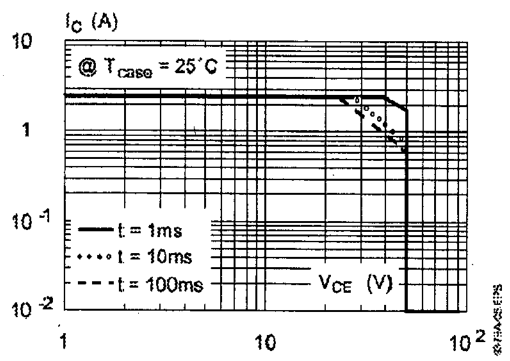
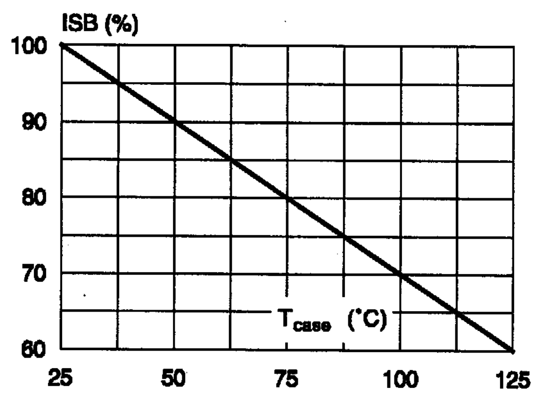


Figure 3. Secondary breakdown Temperature Derating Curve

(ISB = Secondary Breakdown current)



SDA948x, SDA958x
Application Note IC

PIP IV Picture-In-Picture Version B31

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

For the first steps of a successful design-in there are some proposals for the best setting and the necessary SW modifications to enable the full functionality of the device.

Furthermore, the document gives advice regarding several implementation-related topics.

1.1. Recommended and Mandatory Settings

The recommendation ("R") column gives a default value (may be different from power-up-values) which offers best operation in a standard application. However, under special conditions a different setting may be suitable. In the "user-adjustable/remark" column some remarks are given. Furthermore, an "X" indicates values which are TV-dependent or which can be changed after production or during TV operation (e.g. picture format). The mandatory ("M") items are not intended to be user-adjustable and should be set according to this table. Otherwise the IC may not give full performance. All values are given in decimal number format.

Table 1–1: SDA 948x, Type 2 settings

Name	SA	User-adjustable/ Remark	R	M
ACCFIX	0Eh			0
ADLCK	30h			1
ADLCKSEL	30h			1
ADLCKC	30h			1
AGCMD	0Ah	Use 0 or 3 only. 1 or 2 do work correctly, but have disadvantages compared to 0 or 3.	0	
AGCRES	0Ah	Usually not necessary to be set, but may be used manually after change of channel, when AGCMD=0 or 2 is used.	0	
AGCVAL	0Ah	X, only effective if AGCMD=3	8	
BCOROFF	33h		0	
BELLIIR	2Eh		1	
BGFRC	19h	X	0	
BGPOS	0Eh		1	
BGU	18h	X	0	
BGV	19h	X	0	
BGY	17h	X	1	
BLKCVAL	0Bh		0	
BLKINVB	13h		0	
BLKINVR	13h		0	
BLKLB	13h		0	
BLKLG	12h		0	
BLKLR	11h		0	
BLKVCFIL	0Ch		0	
BLKVCHYS	0Bh		0	
BRTADJ	12h	X	8	
CHRBW	0Eh		0	
CKILL	0Dh		0	
CLMCHRY	36h		0	
CLMPID	0Bh		3	
CLMPIST	37h	Back-porch clamping=26 Sync-tip-clamping=3.	26	
CLMSTGY	35h	Back-porch clamping is recommended (CLMSTGY=0). However, sync-tip clamping also works with some clamping noise. Depending on the clamping algorithm, the position of clamping pulse must be set accordingly (CLMPIST).	0	
CLPDEL	09h		0	

Table 1–1: SDA 948x, Type 2 settings, continued

Name	SA	User-adjustable/ Remark	R	M
CLPLEN	21h		7	
CLRANGE	30h		1	
COLON	0Eh		0	
CONADJ	11h	X	8	
CPLLOF	10h			0
CPOS	00h	X	0	
CSTAND	0Dh		0	
CSTDEX	0Dh	X	0	
CVBSEL	0Bh	X	0	
DEEMP	0Eh		0	
DISPMOD	09h	X	0	
DISPSTD	04h		0	
DTECT5060	32h		1	
ENLIM	31h		0	
FIESEL	00h		0	
FILTBRST	37h			1
FLNSTRD	36h		0	
FMACTI	10h		0	
FMACTP	05h		0	
FPSTD	05h		0	
FREEZE	04h	X	0	
FRSEL	07h		1	
FRU	18h		15	
FRV	19h		1	
FRWIDTH	07h		4	
FRWIDV	07h		2	
FRY	17h		3	
HFP	03h		0	
HSHRNK	20h		0	
HSPINV	06h		0	
HUE	0Fh	X	0	
HZOOM	05h	X	0	
IFCOMP	0Fh		2	
INFRM	07h		0	
IRQCON	1Ch	X	0	
ISHFT	31h	Do NOT use ISHFT>0 and PLLTC=0. If PLLTC = 0, ISHFT must be 0 also. If PLLTC > 0, every value for ISHFT is allowed.	3	
LATENCY	37h		3	
LMOFST	0Bh	X	0	
LOCKSP	2Fh		3	
MAT	17h	X	0	
MOSAIC	04h	X	0	
MPIPBG	1Ch		0	
NADJ	30h	X	3	
NOSIGB	0Ah		1	
NSRED	31h	TV: NSRED=4 VCR: NSRED=6. If source not known: All sources: NSRED=6	6	
OUTFOR	18h		0	
PALIDL0	1Dh		1	
PALIDL1	1Dh		1	
PALIDL2	1Dh		1	
PALINC1	2Fh		0	
PALINC2	2Fh		0	
PIPBG	05h	X	0	
PIPBLK	1Dh	X	0	
PIPON	00h		1	
PKBOOST	21h		1	

Table 1–1: SDA 948x, Type 2 settings, continued

Name	SA	User-adjustable/ Remark	R	M
PKLB	16h	X	128	
PKLG	15h	X	128	
PKLR	14h	X	128	
PLLITC	0Ch	TV: PLLITC=2 VCR: PLLITC=0 If source not known: All sources: PLLITC=1	1	
POSCOR	09h	After every new synchronization, set this bit to “1” for a short period of time		0
POSHOR	01h	X	10	
POSOFH	1Eh		0	
POSOFV	1Eh		0	
POSVER	02h	X	20	
PROGEN	00h	0 for interlaced, 1 for progressive display	0	
READD	00h	0 for single-scan, 1 for double-scan display	0	
REFINT	13h		0	
RGBINS	08h	X	0	
SATADJ	1Ah		8	
SATNR	10h		1	
SCADJ	10h	X	10	
SCMIDL	2Eh		5	
SCMREL	2Eh		2	
SECACC	2Fh		1	
SECACCL	2Fh		5	
SECDIV	2Eh		1	
SELDEL	08h	X	12	
SELDOWN	08h		1	
SELLNR	1Ch		1	
SERVICE	1Ch		0	

Table 1–1: SDA 948x, Type 2 settings, continued

Name	SA	User-adjustable/ Remark	R	M
SIZEHOR	04h	X	1	
SIZEVER	04h	X	1	
SLLTHD	31h		0	
SLLTHDV	35h		6	
SLLTHDVP	35h		0	
TRIOUT	13h		0	
UVPOLAR	18h		0	
UVSEQ	1Ch		0	
VDETIFS	36h		0	
VDETITC	36h		0	
VERBLK	08h	(malfunction)		0
VFLYWHL	35h		1	
VFLY-WHLM	35h		1	
VFP	03h		0	
VLP	36h		1	
VSHRNK	1Fh		0	
VSPDEL	06h	X (application-specific)	10	
VSPINV	06h		0	
VSPNSRQ	06h		1	
VSPRED	07h	X	0	
VTHRH50	34h		8	
VTHRH60	34h		13	
VTHRL50	32h		65	
VTHRL60	33h		60	
XDSCLS	1Bh	X	0	
XDSTPE	1Bh	X	0	
YCDEL	0Ch		0	
YCOR	1Ah		1	
YPEAK	1Ah	X	5	
YUVSEL	00h	X	0	

Table 1–2: Additional SDA9489, SDA9589 settings

Name	SA	User-adjustable/ Remark	R	M
ABRSPD	22h		0	
ABRTHD	22h		0	
CHRADR	26h	X	0	
CHRBGON	25h		0	
CHRBGY	25h		0	
CHRCLR	26h		0	
CHRCOD	26h	X	0	
CHRDHW	25h		0	
CHRFRC	25h	X	1	
CHRY	25h		1	
CZMEN	24h		0	
CZMSP	24h		0	
DISPMOD	23h	X	17	
DWCOR	21h		1	
INFRMOD	23h		0	
OSDON	26h	X	0	
PIPHLT	21h		0	
WIPESP	23h		1	
WRPOS	24h	X	0	

SDRAM 64Mb H-die (x4, x8, x16)
4M x 4Bit x 4 / 2M x 8Bit x 4 / 1M x 16Bit x 4 Banks SDRAM

FEATURES
- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The K4S640432H / K4S640832H / K4S641632H is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 4 bits, / 4 x 2,097,152 words by 8 bits, / 4 x 1,048,576 words by 16 bits, f abricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

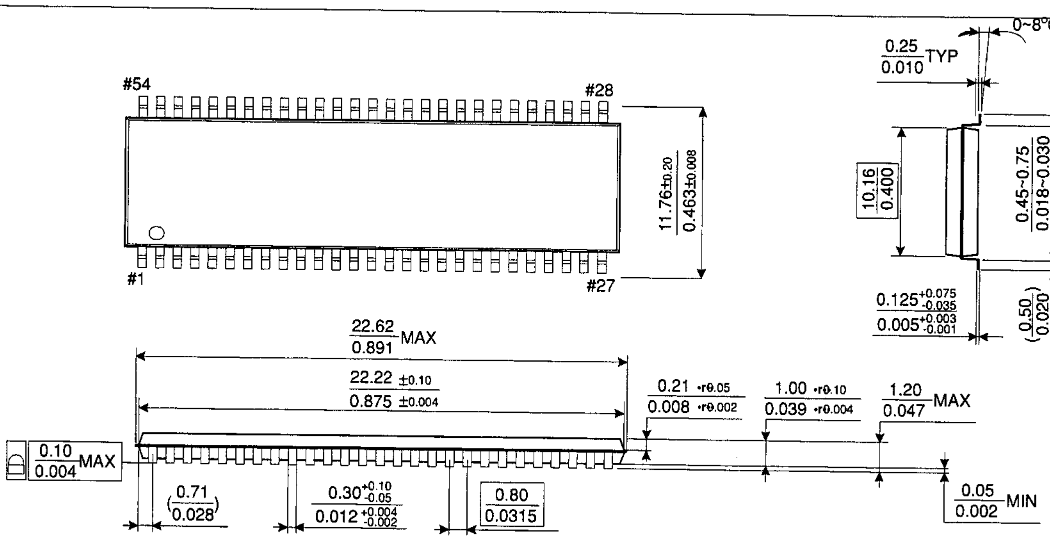
Ordering Information

Part No.	Orgainization	Max Freq.	Interface	Package
K4S640432H-TC(L)75	16Mb x 4	133MHz(CL=3)	LVTTL	54pin TSOP(II)
K4S640832H-TC(L)75	8Mb x 8	133MHz(CL=3)		
K4S641632H-TC(L)60	4Mb x 16	166MHz(CL=3)		
K4S641632H-TC(L)70		143MHz(CL=3)		
K4S641632H-TC(L)75		133MHz(CL=3)		

Organization	Row Address	Column Address
16Mx4	A0~A11	A0-A9
8Mx8	A0~A11	A0-A8
4Mx16	A0~A11	A0-A7

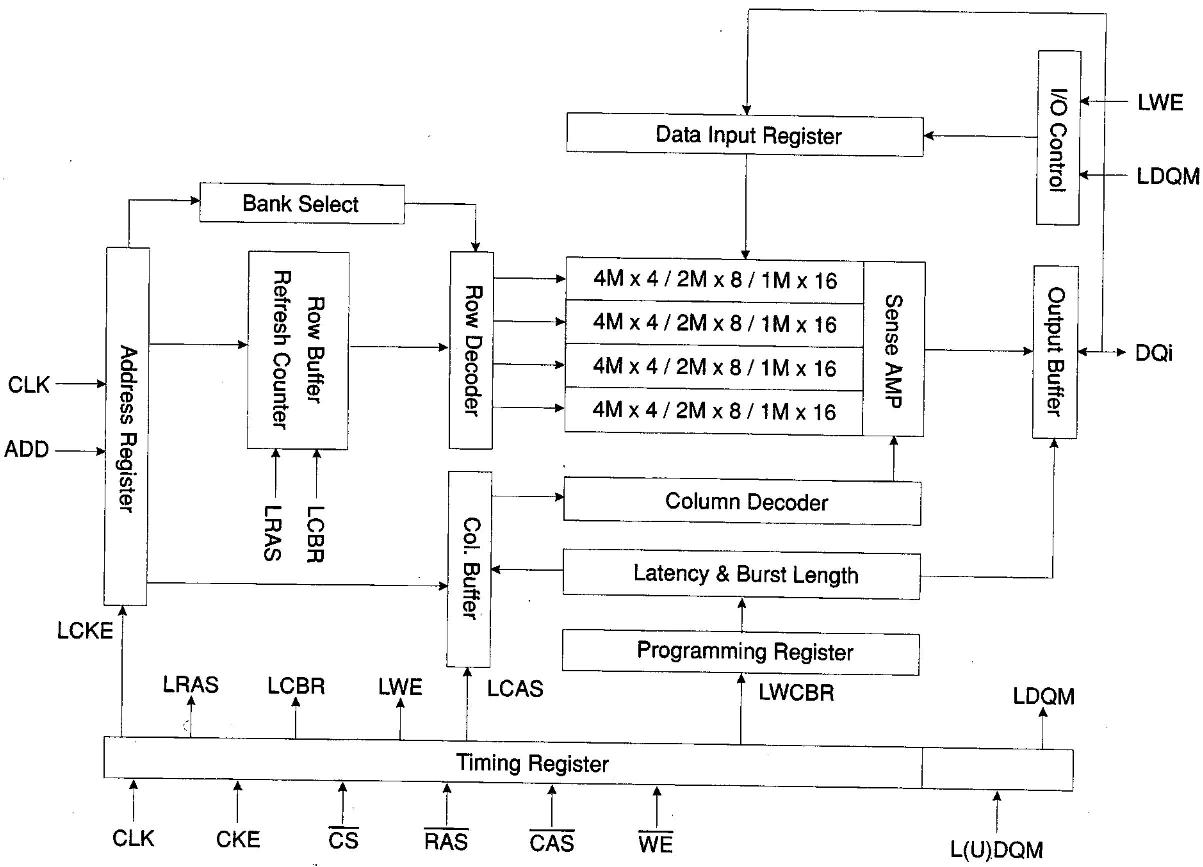
Row & Column address configuration

Package Physical Dimension



54Pin TSOP(II) Package Dimension

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)

x16	x8	x4	Pin	Pin	x4	x8	x16
V_{DD}	V_{DD}	V_{DD}	1	54	V_{SS}	V_{SS}	V_{SS}
DQ0	DQ0	N.C	2	53	N.C	DQ7	DQ15
V_{DDQ}	V_{DDQ}	V_{DDQ}	3	52	V_{SSQ}	V_{SSQ}	V_{SSQ}
DQ1	N.C	N.C	4	51	N.C	N.C	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
V_{SSQ}	V_{SSQ}	V_{SSQ}	6	49	V_{DDQ}	V_{DDQ}	V_{DDQ}
DQ3	N.C	N.C	7	48	N.C	N.C	DQ12
DQ4	DQ2	N.C	8	47	N.C	DQ5	DQ11
V_{DDQ}	V_{DDQ}	V_{DDQ}	9	46	V_{SSQ}	V_{SSQ}	V_{SSQ}
DQ5	N.C	N.C	10	45	N.C	N.C	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
V_{SSQ}	V_{SSQ}	V_{SSQ}	12	43	V_{DDQ}	V_{DDQ}	V_{DDQ}
DQ7	N.C	N.C	13	42	N.C	N.C	DQ8
V_{DD}	V_{DD}	V_{DD}	14	41	V_{SS}	V_{SS}	V_{SS}
LDQM	N.C	N.C	15	40	N.C/RFU	N.C/RFU	N.C/RFU
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	16	39	DQM	DQM	UDQM
$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	17	38	CLK	CLK	CLK
$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	18	37	CKE	CKE	CKE
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	19	36	N.C	N.C	N.C
BA0	BA0	BA0	20	35	A11	A11	A11
BA1	BA1	BA1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	27	28	V_{SS}	V_{SS}	V_{SS}

54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	**System clock**	Active on the positive going edge to sample all inputs.
$\overline{CS}$	**Chip select**	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	**Clock enable**	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
$A_0 \sim A_{11}$	**Address**	Row/column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{11}$, Column address : (x4 : $CA_0 \sim CA_9$, x8 : $CA_0 \sim CA_8$, x16 : $CA_0 \sim CA_7$)
$BA_0 \sim BA_1$	**Bank select address**	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	**Row address strobe**	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	**Column address strobe**	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	**Write enable**	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	**Data input/output mask**	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim N}$	**Data input/output**	Data inputs/outputs are multiplexed on the same pins. (x4 : $DQ_{0 \sim 3}$), (x8 : $DQ_{0 \sim 7}$), (x16 : $DQ_{0 \sim 15}$)
V_{DD}/V_{SS}	**Power supply/ground**	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	**Data output power/ground**	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	**No connection /reserved for future use**	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ASOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f=1MHz, V_{REF} = 1.4V± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.5	4.0	pF	1
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	5.0	pF	2
Address	C_{ADD}	2.5	5.0	pF	2
(x4 : DQ0 ~ DQ3), (x8 : DQ0 ~ DQ7), (x16 : DQ0 ~DQ15)	C_{OUT}	4.0	6.5	pF	3

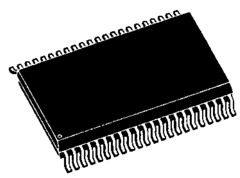
M29KW016E

16 Mbit (1Mb x16, Uniform Block)
3V Supply Light Flash Memory

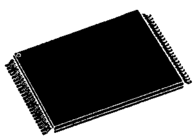
FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Read
  - V_{PP} = 11.4V to 12.6V for Program and Erase
- ACCESS TIME: 90, 110ns
- PROGRAMMING TIME
  - 9µs per Word typical
  - Multiple Word Programming Option (2s typical Chip Program)
- ERASE TIME
  - 11s typical factory Chip Erase
- UNIFORM BLOCKS
  - 8 blocks of 2 Mbits
- PROGRAM/ERASE CONTROLLER
  - Embedded Word Program algorithms
- 10,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code : 88ABh

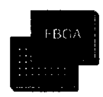
Figure 1. Packages



SO44 (M)



TSOP48 (N)
12 x 20mm



TFBGA48 (ZA)
6 x 9mm

SUMMARY DESCRIPTION

The M29KW016E is a 16 Mbit (1Mb x16) non-volatile memory that can be read, erased and reprogrammed. Read operations can be performed using a single low voltage (2.7 to 3.6V) supply. Program and Erase operations require an additional V_{PP} (11.4 to 12.6) power supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into 8 uniform blocks that can be erased independently so it is possible to preserve valid data while old data is erased (see Figures 2, Block Addresses). Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller (P/E.C.) simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

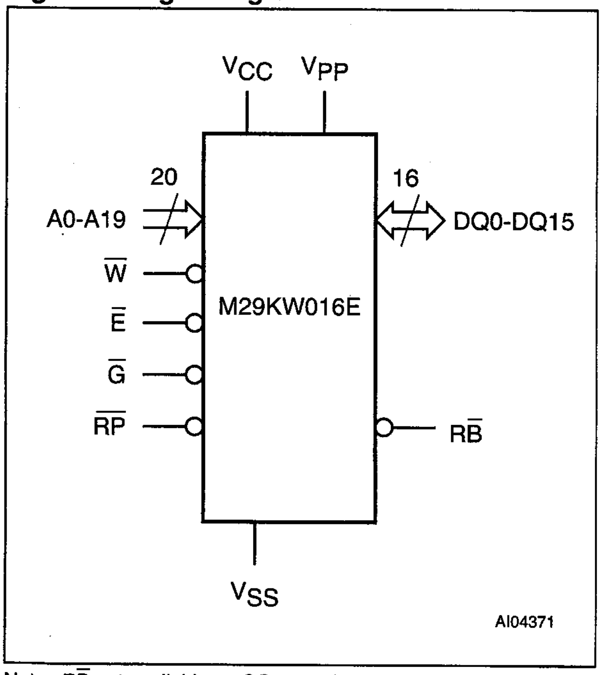
The M29KW016E features a new command, Multiple Word Program, used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written to the memory at any one time. Using this command the entire memory can be programmed in 2s, compared to 9s using the standard Word Program.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in SO44, TSOP48 (12 x 20mm) and TFBGA48 (6 x 9mm, 0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram



Note: $\overline{RB}$ not available on SO44 package.

Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
$R\overline{B}$	Ready/Busy Output (not available on SO44 package)
V_{CC}	Supply Voltage read
V_{PP}	Supply Voltage program erase
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. SO Connections

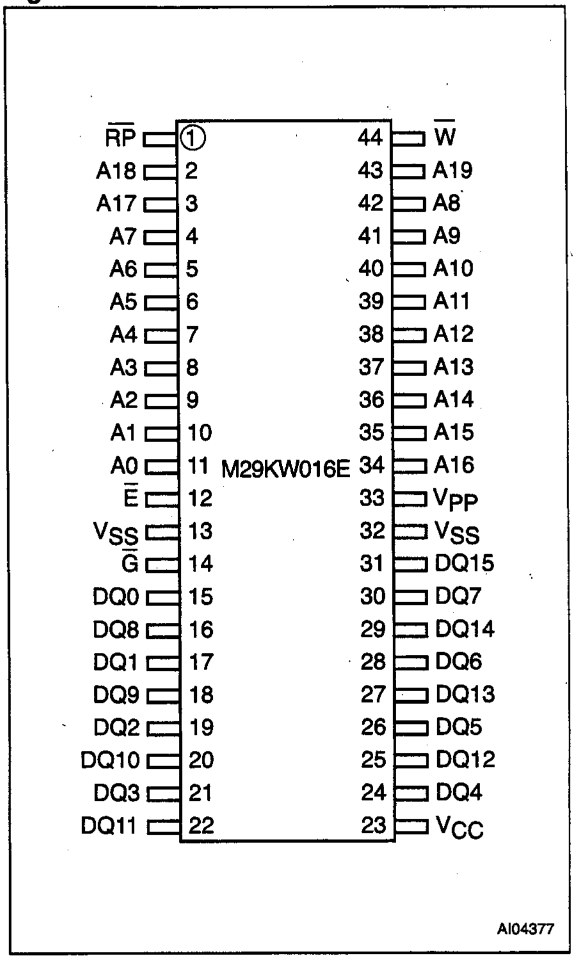
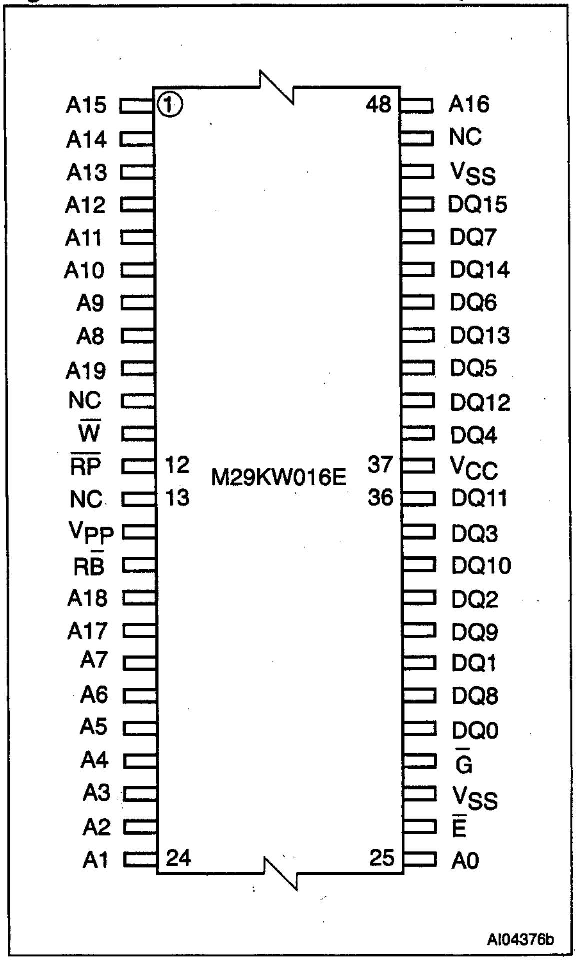


Figure 4. TSOP Connections



TDA9885/V3; TDA9886/V3

I²C-bus controlled single/multistandard alignment-free IF-PLL

FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
- Multistandard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L/L accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz
- 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- External AGC setting via pin 3
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter; AFC bits via I²C-bus readable
- TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled)
- SIF AGC for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- Four I²C-bus addresses via MAD
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module Address (MAD).

GENERAL DESCRIPTION

The TDA9885 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation including sound AM and FM processing.

Both devices can be used for TV, VTR, PC and set-top box applications.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9885T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9886T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4.5	5.0	5.5	V
I_P	supply current		52	63	70	mA
$V_{i(VIF)(rms)}$	VIF input signal voltage sensitivity (RMS value)	–1 dB video at output	–	60	100	μV
$G_{VIF(cr)}$	VIF gain control range	see Fig.10	60	66	–	dB
f_{VIF}	vision carrier operating frequencies	see Table 32	–	33.4	–	MHz
			–	33.9	–	MHz
			–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Fig.7	–	±2.3 –	MHz	
$V_{o(v)(p-p)}$	video output signal voltage (peak-to-peak value)	normal mode; see Fig.9	1.7	2.0	2.3	V
		trap bypass mode; see Fig.9	0.95	1.10	1.25	V
G_{dif}	differential gain	*"CCIR 17"*; note 2				
		B/G standard	–	–	5	%
		L standard	–	–	7	%
φ_{dif}	differential phase	*"CCIR 17"*	–	2	4	deg
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	$C_L < 20$ pF; $R_L > 1$ kΩ; AC load; note 3				
		$f_{trap} = 4.5$ MHz	3.95	4.05	–	MHz
		$f_{trap} = 5.5$ MHz	4.90	5.00	–	MHz
		$f_{trap} = 6.0$ MHz	5.40	5.50	–	MHz
		$f_{trap} = 6.5$ MHz	5.50	5.95	–	MHz
α_{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	–	dB
		B/G standard	30	36	–	dB
S/N_W	weighted signal-to-noise ratio of video signal	see Fig.5; note 4	56	59	–	dB
$PSRR_{17}$	power supply ripple rejection at pin 17	$f_{ripple} = 70$ Hz; video signal; grey level; positive and negative modulation; see Fig.8	20	25	–	dB
$B_{v(-1dB)}$	–1 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ; AC load; trap bypass mode	5	6	–	MHz
AFC_{stps}	AFC steepness $\Delta I_{21}/\Delta f_{VIF}$		0.85	1.05	1.25	μA/kHz
$V_{o(AF)(rms)}$	audio output signal voltage at pin 8 (RMS value)	27 kHz FM deviation; 50 μs de-emphasis	430	540	650	mV
THD_{audio}	total harmonic distortion of audio signal	27 kHz FM deviation; 50 μs de-emphasis	–	0.15	0.50	%
		AM; m = 54% –		0.5	1.0	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$B_{AF(-3dB)}$	−3 dB audio frequency bandwidth for FM	without de-emphasis; dependent on loop Şlter at pin 4	80	100	–	kHz
$S/N_{W(audio)}$	weighted signal-to-noise ratio of audio signal	27 kHz FM deviation; 50 µs de-emphasis; vision carrier unmodulated	52	56	–	dB
		AM; m = 54%	45	50	–	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	50 µs de-emphasis; AM: f = 1 kHz; m = 0.54 referenced to 27 kHz FM deviation	40	46	–	dB
$PSRR_{8(AM)}$	power supply ripple rejection at pin 8	f_{ripple} = 70 Hz; see Fig.8	20	26	–	dB
$PSRR_{8(FM)}$	power supply ripple rejection at pin 8	f_{ripple} = 70 Hz; see Fig.8	14	20	–	dB
$V_{o(rms)}$	IF intercarrier level (RMS value)	QSS mode; SC_1; sound carrier 2 off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; SC_1; sound carrier 2 off	–	note 5	–	mV
f_{ref}	frequency of reference signal at pin 15	note 6	–	4	–	MHz
$V_{ref(rms)}$	amplitude of reference signal source (RMS value)	operation as input terminal	80	–	400	mV

Notes

1. Values of video and sound parameters can be decreased at V_P = 4.5 V.
2. Condition: luminance range (5 steps) 0 to 100%.
3. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 16 to 21; $|H(s)|$ is the absolute value of transfer function).
4. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 17). B = 5 MHz weighted in accordance with *"CCIR 567"*.
5. The intercarrier output signal at pin 12 can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)(rms)} = 1.1\ \text{V (p-p)} \times \frac{1}{2\sqrt{2}} \times 10^{\frac{\frac{V_{i(SC)}}{V_{i(PC)}}(\text{dB}) + 6\ \text{dB} \pm 3\ \text{dB}}{20}}$$

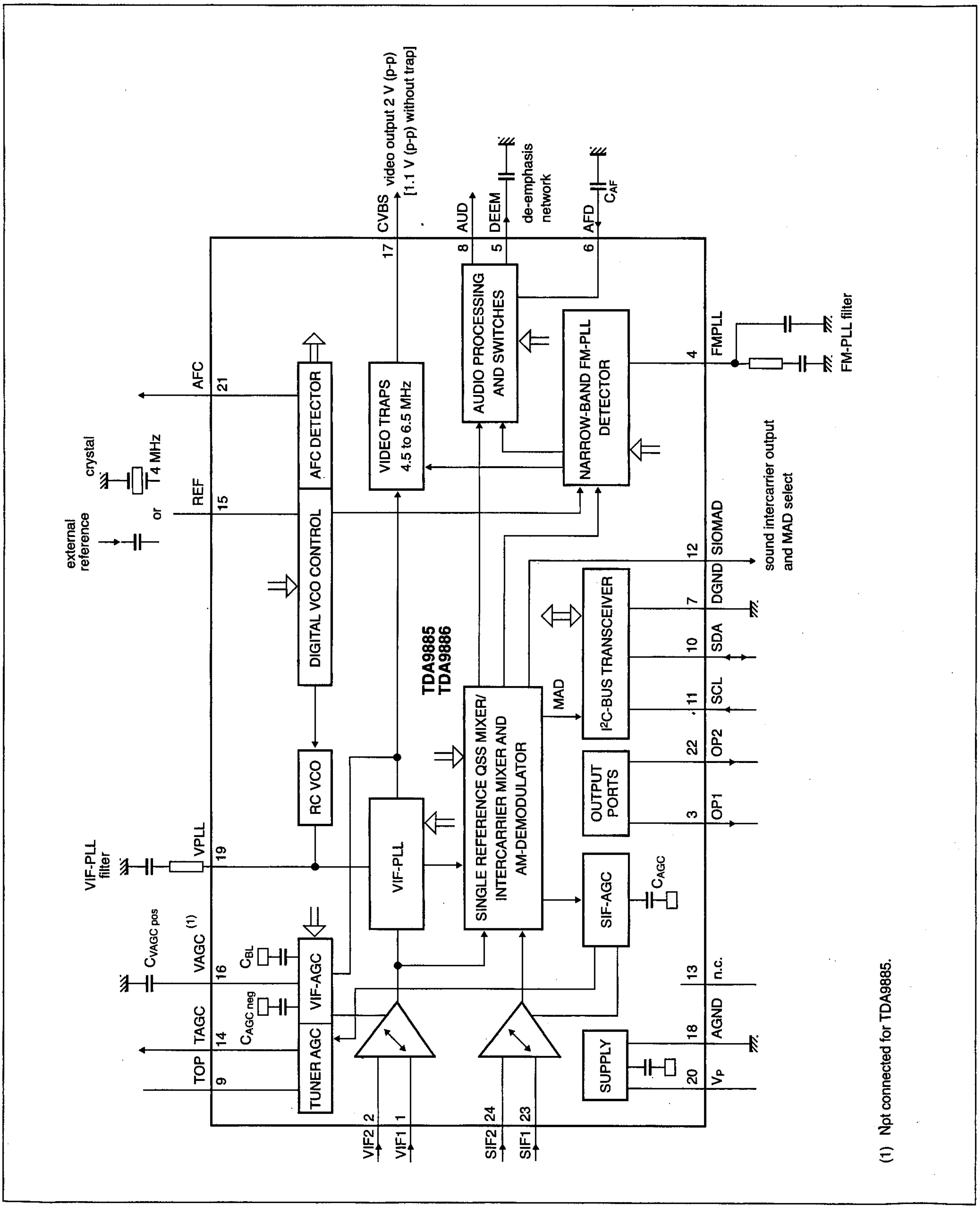
where:

$\frac{1}{2\sqrt{2}}$ = correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(\text{dB})$ = sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB,

6 dB = correction term of internal circuitry and ±3 dB = tolerance of video output and intercarrier output amplitude $V_{o(intc)(rms)}$.

6. The reference input pin 15 is able to operate as a 1-pin crystal oscillator as well as input terminal with external reference signal, e.g. from the tuning system.

BLOCK DIAGRAM



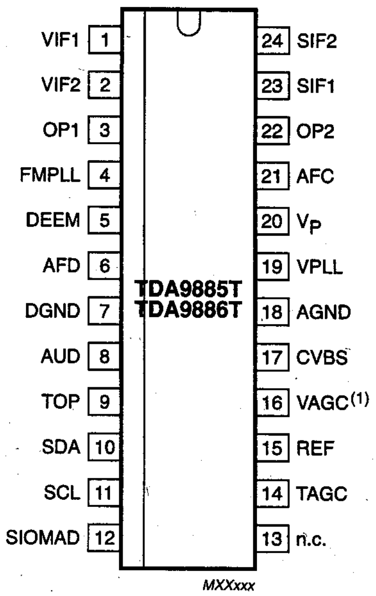
(1) Not connected for TDA9885.

PINNING

SYMBOL	PIN	DESCRIPTION
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
OP1	3	output 1 (open-collector)
FMPLL	4	FM-PLL for loop Şlter
DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
DGND	7	digital ground
AUD	8	audio output
TOP	9	tuner AGC TakeOver Point (TOP)
SDA	10	I²C-bus data input/output
SCL	11	I²C-bus clock input
SIOMAD	12	sound intercarrier output and MAD select
n.c.	13	not connected
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference input
VAGC	16	VIF-AGC for capacitor; note 1
CVBS	17	video output
AGND	18	analog ground
VPLL	19	VIF-PLL for loop Filter
V_P	20	supply voltage (+5 V)
AFC	21	AFC output
OP2	22	output 2 (open-collector)
SIF1	23	SIF differential input 1
SIF2	24	SIF differential input 2

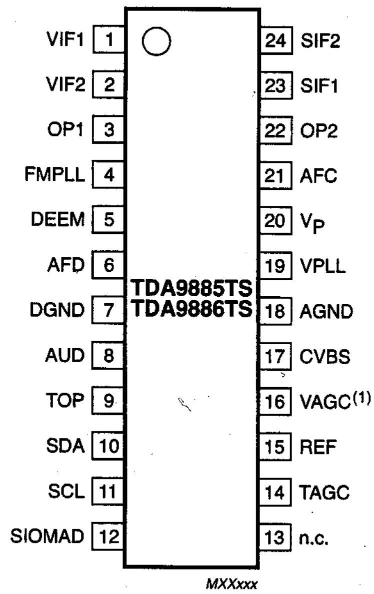
Note

1. Not connected for TDA9885.



(1) Not connected for TDA9885T.

Fig.2 Pin configuration for SO24.



(1) Not connected for TDA9885TS.

Fig.3 Pin configuration for SSOP24.

TEA6415
Audio - Video

I - SUMMARY OF FEATURES

- 2 x SCART CONNECTORS
  SCART 1 : RGB + FB inputs, CVBS input, CVBS output (T V), Stereo audio inputs, stereo audio outputs
  SCART 2 : RGB + FB inputs, CVBS input, CVBS output, Stereo audio inputs, stereo audio outputs
- 2 x EXT CVBS (Cinch) connectors
  Ext CVBS IN, CVBS OUT (Picture In Picture)
- 4 x Stereo audio (Cinch) connectors
  Ext audio IN 1, Ext audio IN 2, Ext audio OUT
  TAPE OUT
- TV AV connections (internal connections)
  TV TUNER : CVBS input, STEREO AUDIO inputs
  To video processor : RGB + FB, Y/CVBS/SYNC, C/CVBS
  To audio processor : Stereo audio outputs
- MCU/PC INTERFACE

2 - INTRODUCTION

In recent years, the selection of hardware available for complete TV systems has grown considerably. Peripherals such as VCRs, laser disc players, camcorders, and home computers are now commonplace on the consumer market. Thus, modern TV receivers are required to control and route many signals between these external peripherals and various internal stages of the set. Therefore it is becoming a standard practise to feature many input and output connections at the rear of the unit (SCART, SVHS, RCA, etc...).

High-end TV sets have extra integrated features such as internal satellite decoders, 2 tuners, picture in picture, HIFI sound, multistandards reception, etc. with menu control of all functions via the remote control.

All these extra signal sources and functions must be handled at the audio/video matrix section of the TV set. The significance and complexity of this stage has been forced to grow in pace with these modern trends, and the use of a microprocessor for control is common place. In parallel with this, the physical size of the TV receiver chassis is required to be minimized. Thus, modern TV receiver designs challenge traditional methods of switching these signals in terms of both economy and technical performance (since it is obvious that a greater number of uncorrelated signals present at this stage produce greater unwanted interaction effects).

The technical performance requirements are further stressed by the evolution of techniques that are intended to enhance both picture and sound quality (SVHS and nicam for example), which require wider bandwidth and lower distortion signal handling.

Conventional designs based on dis crete circuitry or low cost analog CMOS gates are no longer feesible. The market demand is thus for dedicated ICs with optimised performance for handling all the audio and video interconnections under direct microprocessor control.

SGS-THOMSON has answered the demands of the TV industry with the introduction of optimized audio and video matrix products that can be directly controlled by the I^2C bus. The high signal density, performance and flexibility of these components allow them to satisfy a wide range of applications.

3 - GENERAL DESCRIPTION/ARCHITECTURE

This demonstration board attempts to show the versatility, performance and simplicity of an audio/video matrix system that uses only three SGS-THOMSON ICs. The circuit architecture is intended to reflect a typical high-end TV set AV stage with SCART connections (with RGB inputs), SVHS inputs and outputs, internal and external CVBS and stereo audio connections.

Figure 2 shows a simplified circuit schematic of the demo board.

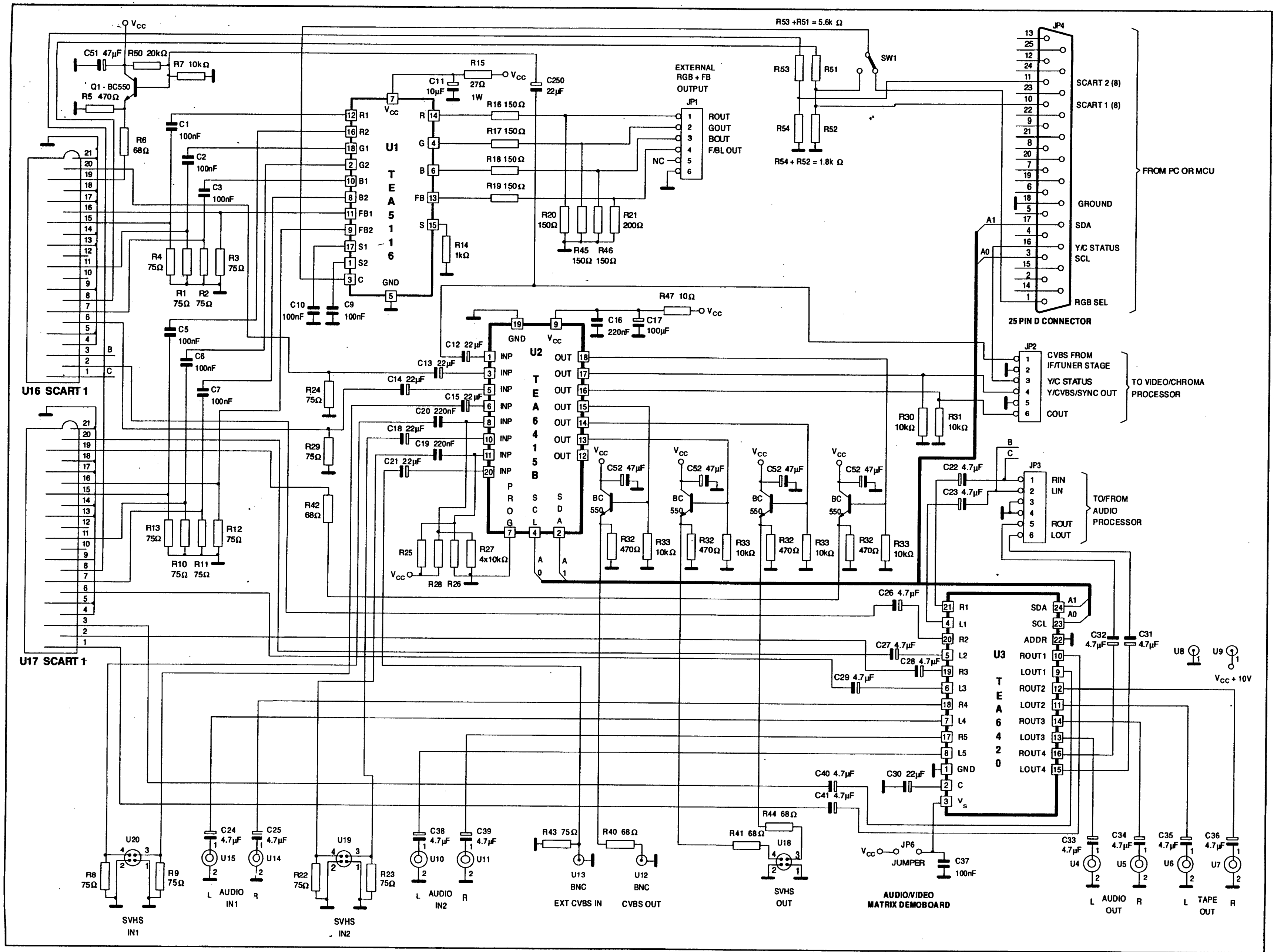
Two SCART sockets are incorporated which deliver two RGB and Fast Blanking signals which are switched by the TEA5116.

All audio connections are handled by the TEA6420 I^2C bus controlled audio matrix. Any of the 5 stereo audio sources can be routed to one or more of 4 stereo outputs with bus programmable gain (from 0 to 6 dB). All remaining video signal switching is performed by the TEA6415B I^2C bus controlled video matrix.

Two SVHS inputs are featured with corresponding audio inputs. The Y/C components connect to 4 of the TEA6415B inputs, and an SVHS output socket is included which can receive one of these Y/C sources. An extra EXT CVBS IN (BNC connection) is featured to complete the video matrix inputs. This function is useful for Y + C mix requirements (see applications section Figure 4). The video matrix outputs connect to the TV output (LUMA + CHROMA), SCART 2 CVBS out, SVHS output (LUMA + CHROMA), and an external CVBS OUT (BNC connection), which can be employed as the PIP output.

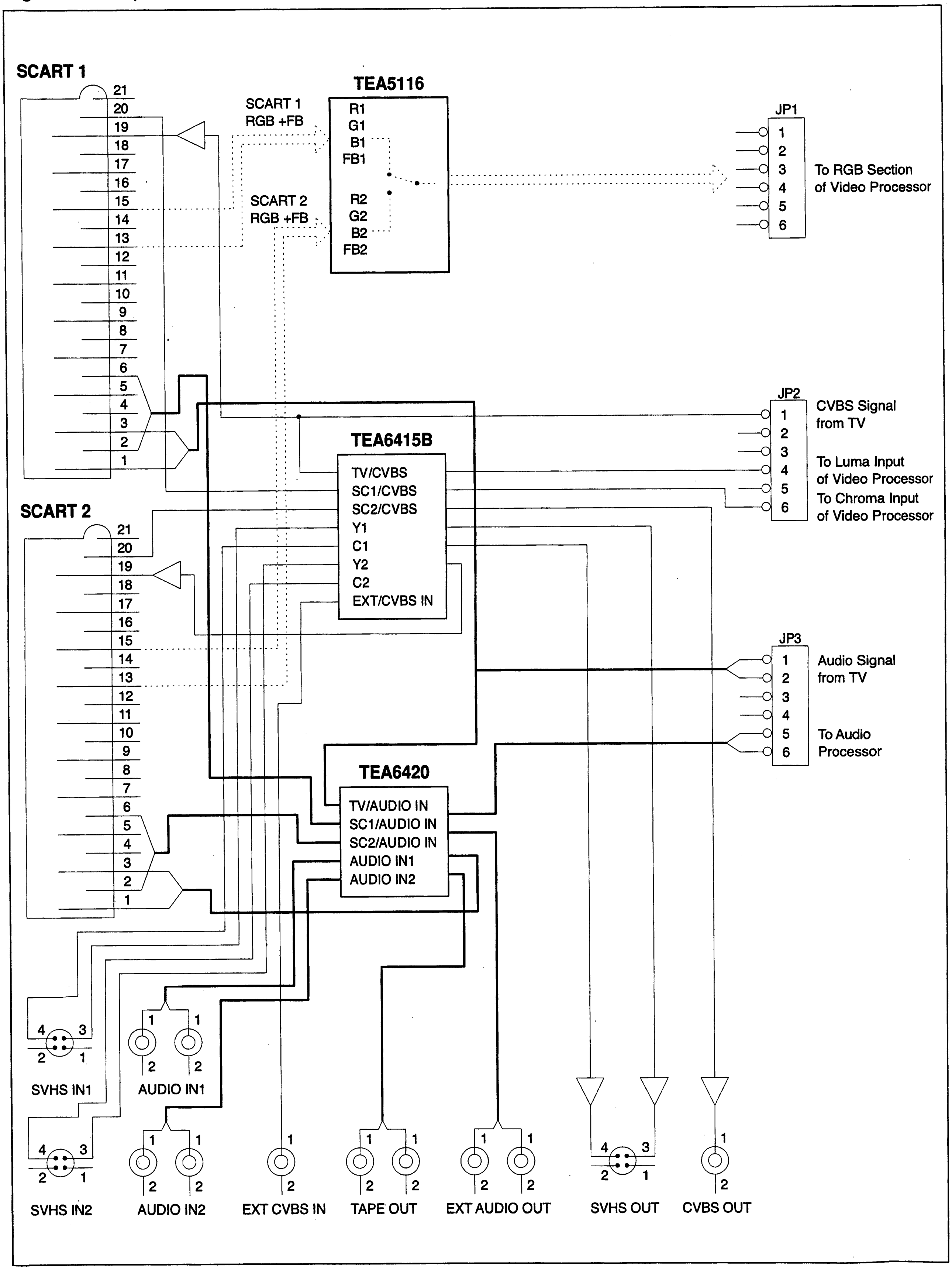
The audio matrix (TEA6420) handles all the peripheral stereo audio inputs plus the TV IF sound. Two pairs of outputs are connected by CINCH - one AUDIO OUT which is to be used in conjunction with SVHS OUT or CVBS OUT ; the other audio output pair is labelled TAPE OUT for direct sound recording or HIFI connection.

Figure 1 : AV Demoboard detailed Electric Schematic



AN632-01.EPS

Figure 2 : Simplified AV Board Schematic



4 - APPLICATION

4.1 - TV Connections

Figure 3 shows the suggested method for connection of the AV Demo Board to the appropriate stages of a TV receiver.

4.1.a - AV board input signals from TV IF stage

The CVBS signal from the TV receiver's IF stage must be connected to the AV board at JP2 pin 1. The corresponding stereo audio signals are to be connected to JP3 pins 1 (stereo Right) and 2 (stereo Left).

4.1.b - AV board output signals to video/chroma processor

The AV board TV video output signals are connected on JP1 and JP2. JP1 has the RGB+Fb component outputs on pins 1,2,3, and 4 respectively. Usually, these signals connect directly to the video processor, since it has internal RGB switching to accommodate the external RGB source and TEXT RGB. However if this switching has to be performed externally to the video processor, an RGB+FB switch IC (TEA5114A or TEA5115) could be used. In this case, R21 should be increased to 300Ω.

JP2 connects the video matrix outputs to the TV. It must be noted that these signals are amplified (X2) at this point. Pin 4 must be connected to the luma signal processing circuit, and pin 6 to the chroma processing circuit. The total load impedance on the video matrix outputs must not be less than 3k, (note that characterisation was performed with the 10k loads supplied on the pcb). When the AV board is used in conjunction with the supplied PC software, a Y/C STATUS flag is output on pin 3. Three cases must be considered as follows :

(a) when an SVHS source is selected in the TV DISPLAY MENU, the Y signal is routed to JP2 pin 4 and the C signal to pin 6. The Y/C STATUS flag on pin 3 is a logic 0 in this case. The purpose of this function is to initiate control logic which can be used to bypass chroma traps (and consequently increase the luma bandwidth) when processing SVHS signals.

(b) when a CVBS source is selected, it appears at both outputs (pin 4 and pin 6). The Y/C STATUS is a logic 1 (+5V) in this case.

(c) when an RGB source is selected, the corresponding SYNC signal appears at both outputs (pin 4 and pin 6). The Y/C STATUS is a logic 1 (+5V) in this case also.

4.1.c - AV board outputs to audio processor

JP3 connects the stereo audio outputs to the TV audio processor.
Pin 5 is stereo Right and pin 6 is stereo Left.

4.1.d - AV board PICTURE IN PICTURE output

The CVBS OUT (BNC) can be employed for PIP applications. The demonstration software has a dedicated menu to select different CVBS sources for the PIP display.
Two SCART sockets are incorporated which deliver two RGB and Fast Blanking signals which are switched by the TEA5116.
All audio connections are handled by the TEA6420 I^2C bus controlled audio matrix. Any of the 5 stereo audio sources can be routed to one or more of 4 stereo outputs with bus programmable gain from (0 to 6dB). All remaining video signal switching is performed by the TEA6415B I^2C bus controlled video matrix.

Two SVHS inputs are featured with corresponding audio inputs. The Y/C components connect to 4 of the TEA6415B inputs, and an SVHS output socket is included which can receive one of these Y/C sources. An extra EXT CVBS IN (BNC connection) is featured to complete the video matrix inputs. This function is useful for Y + C mix requirements (see applications section Figure 4). The video matrix outputs connect to the TV output (LUMA + CHROMA), SCART 2 CVBS out, SVHS output (LUMA + CHROMA), and an external CVBS OUT (BNC connections), which can be employed as the PIP output.
The audio matrix (TEA6420) handles all the peripheral stereo audio inputs plus the TV IF sound. Two pairs of outputs are connected by CINCH - one AUDIO OUT which is to be used in conjunction with SVHS OUT or CVBS OUT ; the other audio output pair is labelled TAPE OUT for direct sound recording or HIFI connection.

Figure 3 : AV Demoboard Connections to TV Receiver

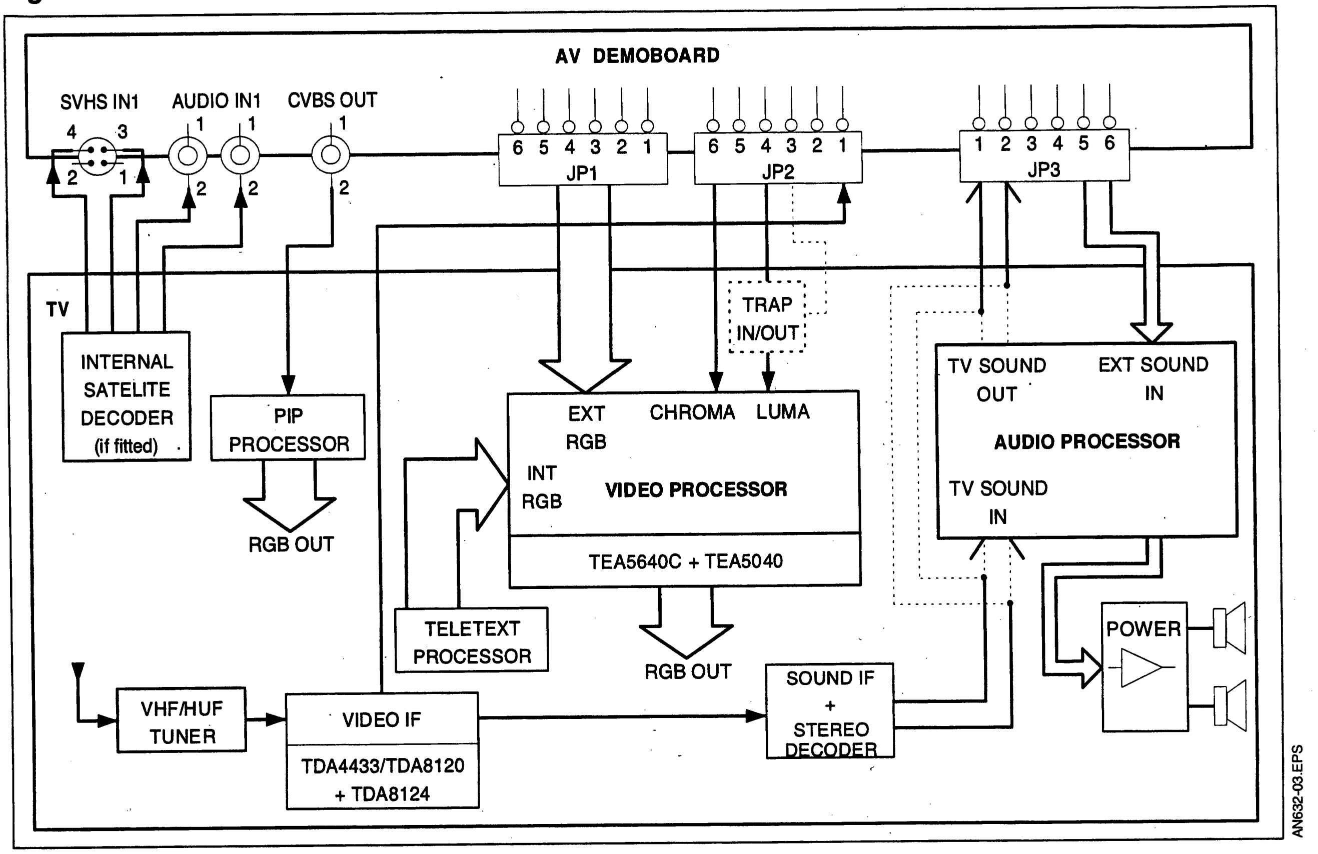
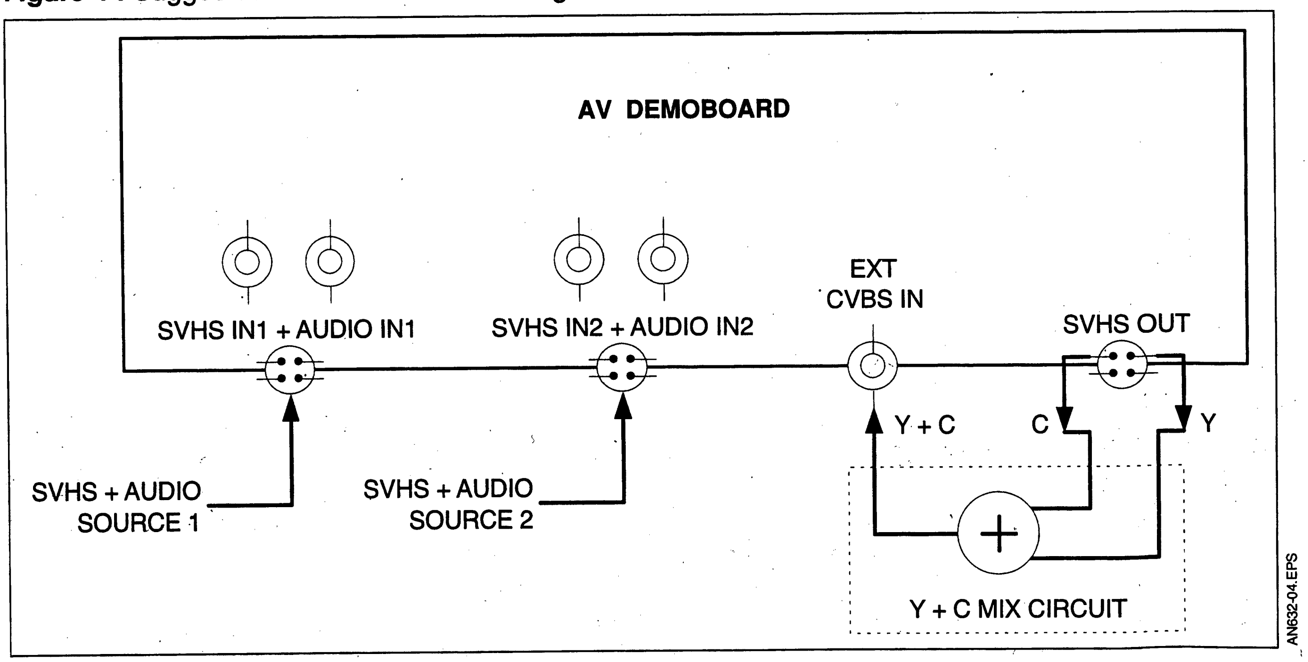


Figure 4 : Suggested Method for Y + C Mixing Function



TDA933xH series
I^{2}C-bus Controlled TV Display Processors

- Can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications
- YUV input and linear RGB input with fast blanking
- Separate OSD/text input with fast blanking or blending
- Black stretching of non-standard luminance signals
- Switchable matrix for the colour difference signals
- RGB control circuit with Continuous Cathode Calibration (CCC), plus white point and black level offset adjustment
- Blue stretch circuit which offsets colours near white towards blue
- Internal clock generation for the deflection processing, which is synchronized by a 12 MHz ceramic resonator oscillator
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Slow start and slow stop of the horizontal drive pulses
- Low-power start-up option for the horizontal drive circuit
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Vertical and horizontal geometry processing
- Horizontal and vertical zoom possibility and vertical scroll function for application with 16 : 9 picture tubes
- Horizontal parallelogram and bow correction
- I^{2}C-bus control of various functions
- Low dissipation.

GENERAL DESCRIPTION

The TDA933xH series are display processors for 'High-end' television receivers which contain the following functions:

- RGB control processor with Y, U and V inputs, a linear RGB input for SCART or VGA signals with fast blanking, a linear RGB input for OSD and text signals with a fast blanking or blending option and an RGB output stage with black current stabilization, which is realized with the CCC (2-point black current measurement) system.
- Programmable deflection processor with internal clock generation, which generates the drive signals for the horizontal, East-West (E-W) and vertical deflection. The circuit has various features that are attractive for the application of 16 : 9 picture tubes.
- The circuit can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications.

In addition to these functions, the TDA9331H and TDA9332H have a multi-sync function for the horizontal PLL, with a frequency range from 30 to 50 kHz ($2f_H$ mode) or 15 to 25 kHz ($1f_H$ mode), so that the ICs can also be used to display SVGA signals.

The supply voltage of the ICs is 8 V. They are each contained in a 44-pin QFP package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9330H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
TDA9331H			
TDA9332H			

SURVEY OF IC TYPES

IC VERSION	VGA MODE	DAC OUTPUT
TDA9330H	no	I^2C-bus controlled
TDA9331H	yes	proportional to VGA frequency
TDA9332H	yes	I^2C-bus controlled

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage	–	8.0	–	V
I_P	supply current (V_{P1} plus V_{P2})	–	50	–	mA
Input voltages					
$V_{i(Y)(b\text{-}w)}$	luminance input signal (black-to-white value)	–	1.0/0.315	–	V
$V_{i(U)(p\text{-}p)}$	U input signal (peak-to-peak value)	–	1.33	–	V
$V_{i(V)(p\text{-}p)}$	V input signal (peak-to-peak value)	–	1.05	–	V
$V_{i(RGB)(b\text{-}w)}$	RGB input signal (black-to-white value)	–	0.7	–	V
$V_{i(Hsync)}$	horizontal sync input (H_D)	–	TTL	–	V
$V_{i(Vsync)}$	vertical sync input (V_D)	–	TTL	–	V
$V_{i(IIC)}$	I^2C-bus inputs (SDA and SCL)	–	CMOS 5 V	–	V
Output signals					
$V_{o(RGB)(b\text{-}w)}$	RGB output signal amplitude (black-to-white value)	–	2.0	–	V
$I_{o(hor)}$	horizontal output current	–	–	10	mA
$I_{o(ver)(p\text{-}p)}$	vertical output current (peak-to-peak value)	–	0.95	–	mA
$I_{o(EW)}$	E-W drive output current	–	–	1.2	mA

BLOCK DIAGRAM

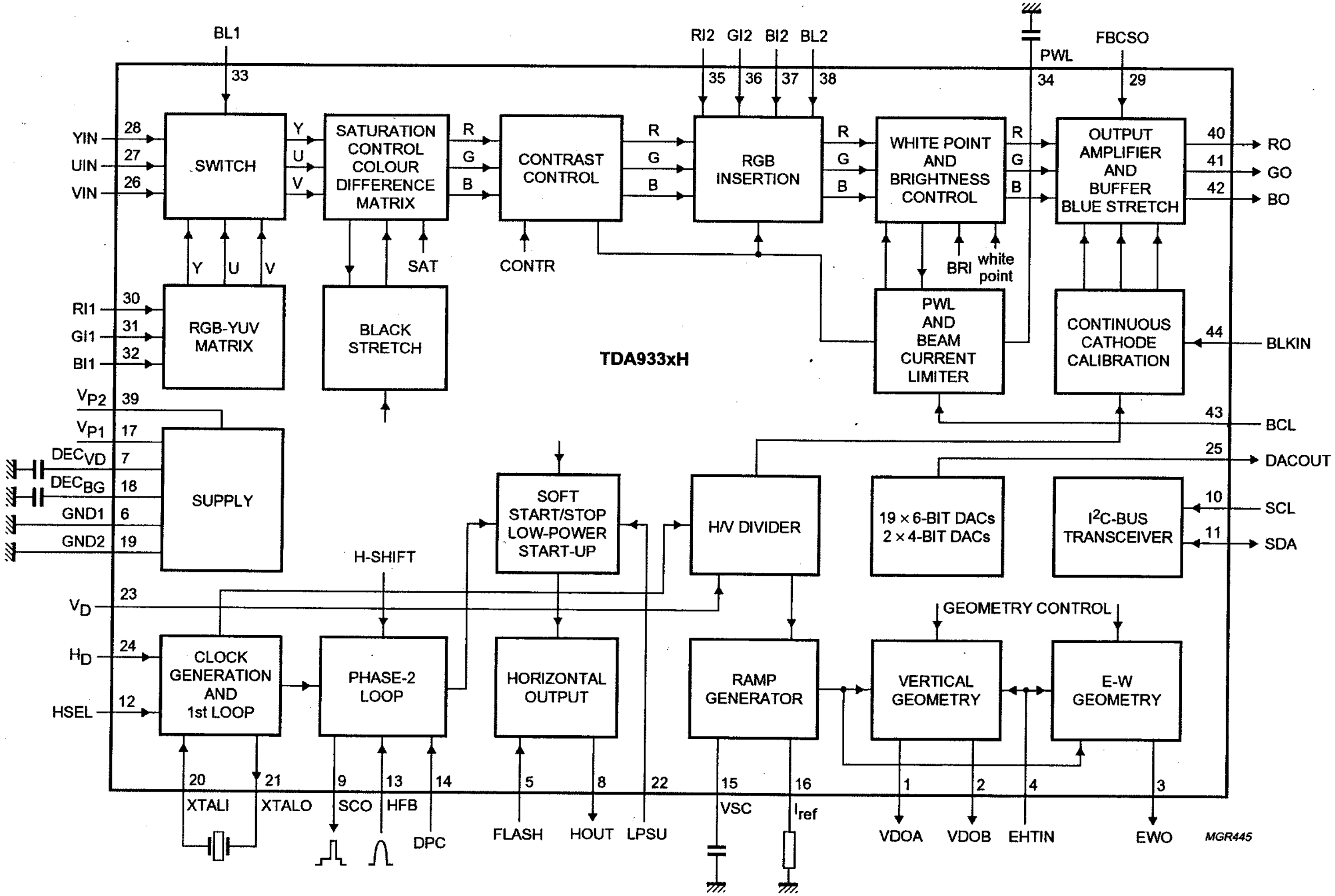
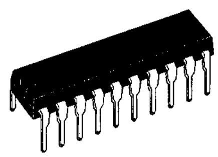


Fig.1 Block diagram.

TDA7480
10W Mono Class-D Amplifier

- 10W OUTPUT POWER: $R_L = 8\Omega/4\Omega$; THD = 10%
- HIGH EFFICIENCY
- NO HEATSINK
- SPLIT SUPPLY
- OVERVOLTAGE PROTECTION
- ST-BY AND MUTE FEATURES
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION



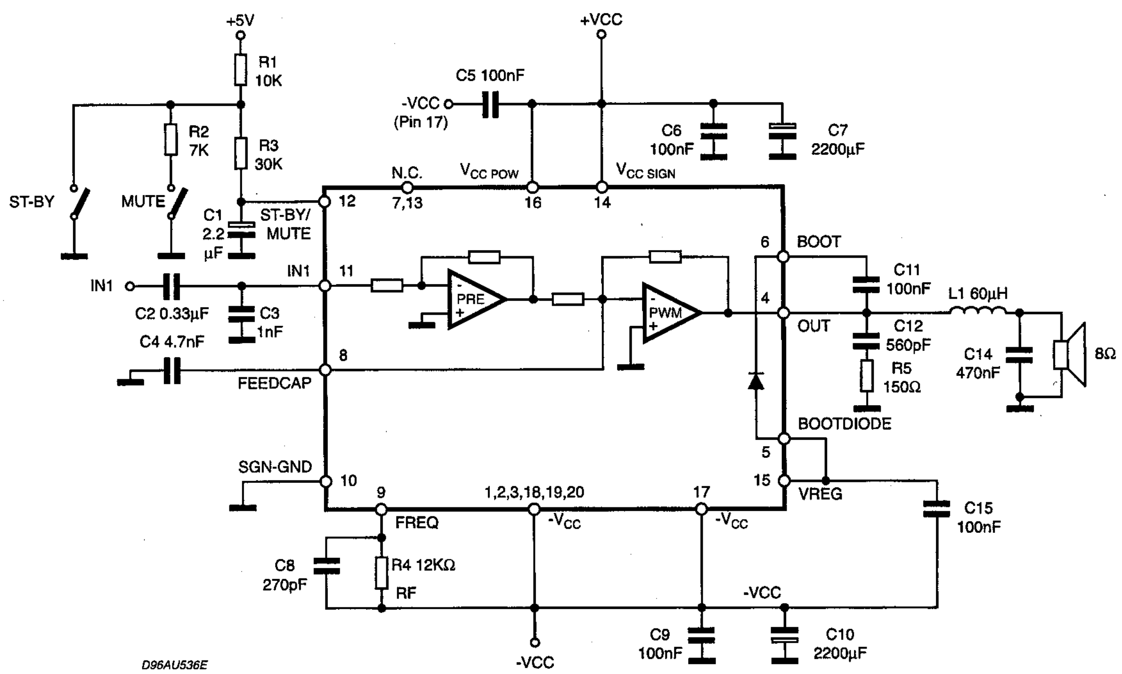
PDIP20 (14+3+3)

ORDERING NUMBER: TDA7480

DESCRIPTION

The TDA7480 is an audio class-D amplifier assembled in Power DIP package specially designed for high efficiency applications mainly for TV and Home Stereo sets.

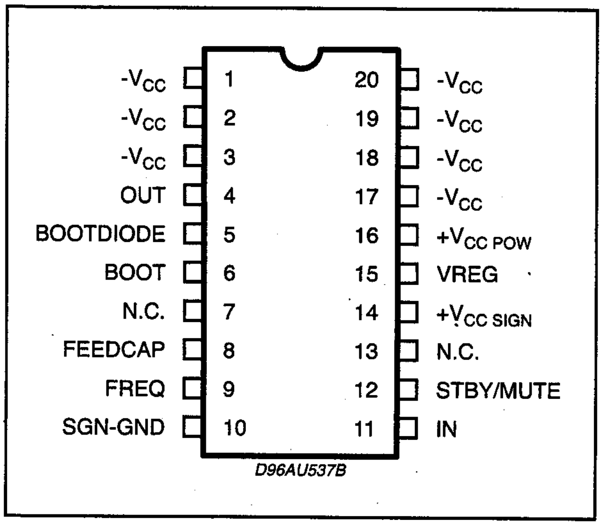
Figure 1: Test and Application Circuit.



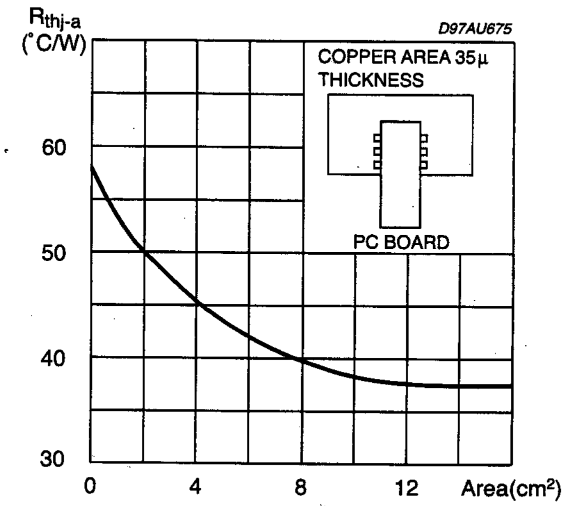
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	±20	V
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C
V_{FREQ}	Maximum Voltage Across VFREQ (Pin 9)	8	V
T_{op}	Operating Temperature Range	-20 to 70	°C
ESD	Maximum ESD on Pins	±1.8	kV

PIN CONNECTION (Top view)



Rth with "on board" Square Heatsink vs. copper area.



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to ambient	80	°C/W
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction to Pin Max.	12	°C/W

PIN FUNCTIONS

N.	Name	Function
1	-V_{CC}	NEGATIVE SUPPLY.
2	-V_{CC}	NEGATIVE SUPPLY.
3	-V_{CC}	NEGATIVE SUPPLY.
4	OUT	PWM OUTPUT
5	BOOTDIODE	BOOTSTRAP DIODE ANODE
6	BOOT	BOOTSTRAP CAPACITOR
7	NC	NOT CONNECTED
8	FEEDCAP	FEEDBACK INTEGRATING CAPACITANCE
9	FREQUENCY	SETTING FREQUENCY RESISTOR
10	SGN-GND	SIGNAL GROUND
11	IN	INPUT
12	ST-BY-MUTE	ST-BY/ MUTE CONTROL PIN
13	NC	NOT CONNECTED
14	+V_{CC} SIGN	POSITIVE SIGNAL SUPPLY
15	VREG	10V INTERNAL REGULATOR
16	+V_{CC} POW	POSITIVE POWER SUPPLY
17	-V_{CC}	NEGATIVE SUPPLY (TO BE CONNECTED TO PIN 16 VIA C5)
18	-V_{CC}	NEGATIVE SUPPLY
19	-V_{CC}	NEGATIVE SUPPLY
20	-V_{CC}	NEGATIVE SUPPLY

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_{CC} = \pm14V$; $R_L = 8\Omega$; $R_S = 50\Omega$; $R_f = 12K\Omega$; Demod.. filter L = 60µH, C = 470nF; f = 1KHz; $T_{amb} = 25°C$ unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		±10		±16	V
I_q	Total Quiescent Current	$R_L = \infty$; NO LC Filter		25	40	mA
V_{OS}	Output Offset Voltage	Play Condition	–50		+50	mV
P_O	Output Power	THD = 10% THD = 1%	8.5 6	10 7		W W
		$R_L = 4\Omega$ $V_{CC} = \pm10.5V$ THD = 10% THD = 1%		 10 7		 W W
P_d (*)	Dissipated Power at 1W Output Power	$R_f = 12K\Omega$ $P_O = 1W$		1		W
P_{DMAX}	Maximum Dissipated Power	$P_O = 10W$ THD 10% $R_{th\text{-}j\text{-}amb} = 38°C/W$ (Area 12cm²)		1.8		W
η	Efficiency $\equiv \frac{P_O}{P_O + P_D} \equiv \frac{P_O}{P_I}$ (**)	THD 10% $R_{th\text{-}j\text{-}amb} = 38°C/W$ (Area 12cm²)	80	85		%
THD	Total Harmonic Distortion	$R_L = 8\Omega$; $P_O = 0.5W$		0.1		%
I_{max}	Overcurrent Protection Threshold	$R_L = 0$	3.5	5		A
T_j	Thermal Shut-down Junction Temperature			150		°C
G_V	Closed Loop Gain		29	30	31	dB
e_N	Total Input Noise	A Curve f = 20Hz to 22KHz		7 12		µV µV
R_i	Input Resistance		20	30		KΩ
SVR	Supply Voltage Rejection	f = 100Hz; $V_r = 0.5$	46	60		dB
T_r, T_f	Rising and Falling Time			50		ns
R_{DSON}	Power Transistor on Resistance			0.4		Ω
F_{SW}	Switching Frequency		100	120	140	KHz
F_{SW_OP}	Switching Frequency Operative Range		100		200	KHz
B_F	Zero Signal Frequency Constant (***)			1.4×10^9		HzΩ
R_F	Frequency Controller Resistor Range (****)		7	12	14	KΩ
MUTE & STAND-BY FUNCTIONS						
$V_{ST\text{-}BY}$	Stand-by range				0.8	V
V_{MUTE}	Mute Range		1.8		2.5	V
V_{PLAY}	Play Range (1)		4			V
A_{MUTE}	Mute Attenuation		60	80		dB
$I_{qST\text{-}BY}$	Quiescent Current @ Stand-by			3	5	mA

*: The output average power when the amplifier is playing music can be considered roughly 1/10 of the maximum output power. So it is useful to consider the dissipated power in this condition for thermal dimensioning.

**: P_O = measured across the load using the following inductor:
COIL 58120 MPPA2 (magnetics) TURNS: 28 ∅ 1mm
COIL77120 KOOL Mµ (magnetics) TURNS: 28 ∅ 1mm

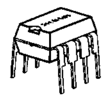
***: The zero-signal switching frequency can be obtained using the following expression: $F_{SW} = B_F/R_F$

****: The maximum value of R_F is related to the maximum possible value for the voltage drop on R_F itself.

(1): For V_{12} >5.2V, an input impedance of 10KΩ is to be considered.

ICE1QS01

Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction (PFC)



P-DIP-8-4

P-DSO-8-3

Features

- Line Current Consumption with PFC
- Standby Input Power < 1 W
- Stable Standby Frequency
- Low Power Consumption
- Very Low Start-up Current
- Soft-Start for noiseless Start-up
- Standby Burst Mode with and without Control Signal for lowered Output Voltages
- Digital Frequency Reduction in small Steps at Decreasing Load
- Over- and Undervoltage Lockout
- Switch Off at Mains Undervoltage
- Mains Voltage Dependent Fold Back Point Correction
- Ringing Suppression Time Controlled from Output Voltage
- Easy Design In
- Free usable Fault Comparator

Functional Description

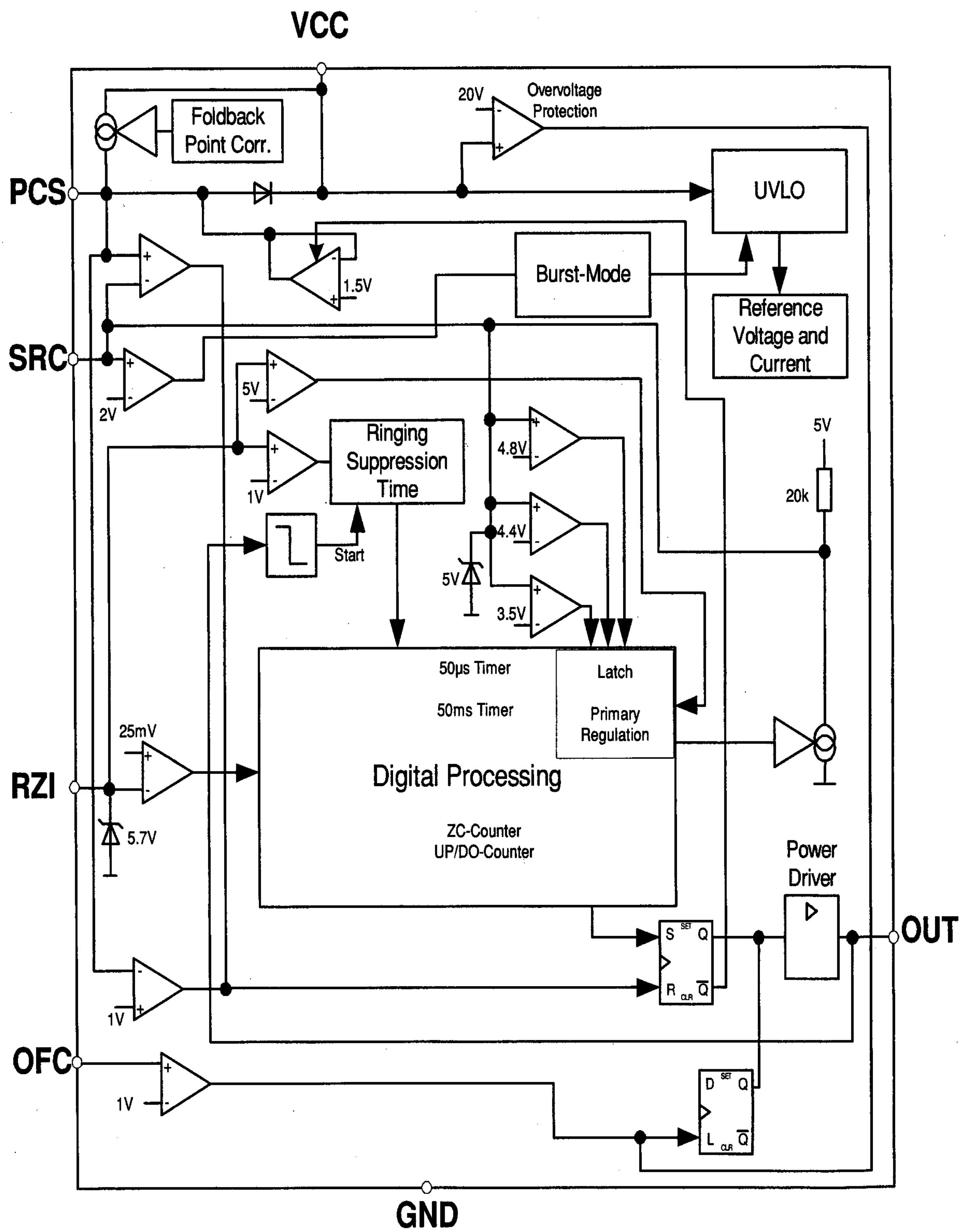
The ICE1QS01 is optimized to control free running flyback converters with and without Power Factor Correction (with PFC Charge Pump).

The switching frequency is reduced in small steps with decreasing load towards a minimum of 20 kHz in standby mode. This function is performed by a digital circuit to avoid any jitter also with periodically pulsed loads. To provide extremely low power consumption at light loads, this device can be switched into Standby Burst Mode. This is also possible without standby control signal (for adapter application).

Additionally, the start up current is very low. To avoid switching stresses of the power devices, the power transistor is always switched on at minimum voltage. The device has several protection functions: V CC over- and undervoltage, mains undervoltage and current limiting. Regulation can be done by using the internal error amplifier or an opto coupler feedback. The output driver is ideally suited for driving a power MOSFET.

The ICE1QS01 is suited for TV-sets, VCR- sets, SAT- receivers and other consumer applications in the power range from 0 to app. 300 W.

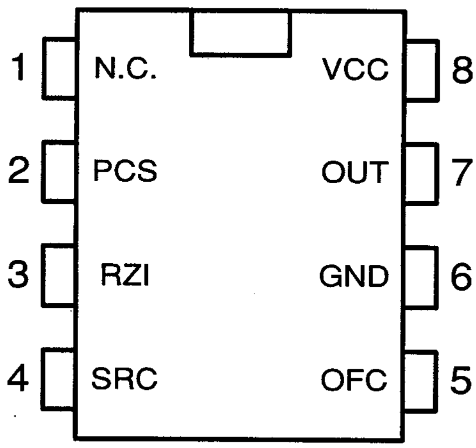
Type	Ordering Code	Package
ICE1QS01	Q67040-S4558-A101	P-DIP-8
ICE1QS01G	Q67040-S4559-A101	P-DSO-8

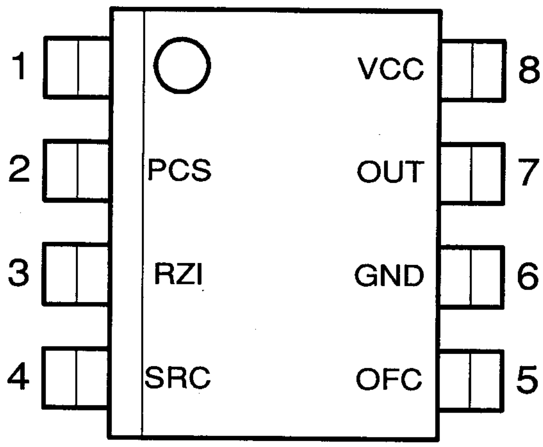

VCC
Foldback
Point Corr.
20V
Overvoltage
Protection
PCS
UVLO
1.5V
Burst-Mode
Reference
Voltage and
Current
SRC
2V
5V
Ringing
Suppression
Time
1V
4.8V
4.4V
Start
5V
3.5V
5V
20k
50µs Timer
50ms Timer
Latch
Primary
Regulation
25mV
RZI
Digital Processing
5.7V
ZC-Counter
UP/DO-Counter
Power
Driver
OUT
1V
OFC
1V
GND

Pinning

Pin	Symbol	Function
1	N.C.	
2	PCS	Primary Current Simulation
3	RZI	Regulation and Zero Crossing Input
4	SRC	Soft-Start and Regulation Capacitor
5	OFC	Overvoltage Fault Comparator
6	GND	Ground
7	OUT	Output
8	VCC	Supply Voltage

Pin Configuration (top view)





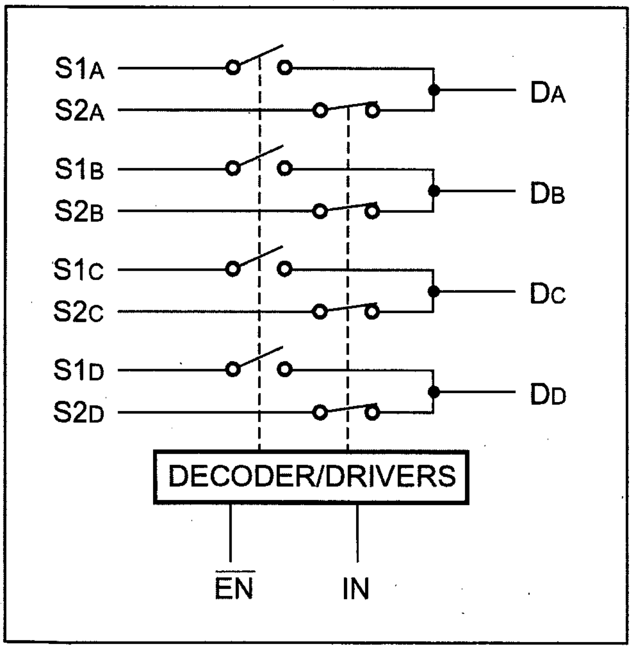
P15V330

Low ON-Resistance Wideband/Video Quad 2-Channel MUX/DEMUX

Product Features:

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: –58 dB
- Ultra-low quiescent power (0.1 μA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
  - 16-pin 300-mil wide plastic SOIC (S)
  - 16-pin 150-mil wide plastic SOIC (W)
  - 16-pin 150-mil wide plastic QSOP (Q)

Functional Block Diagram



Truth Table

EN	IN	ON Switch
0	0	S1A, S1B, S1C, S1D
0	1	S2A, S2B, S2C, S2D
1	X	Disabled

Product Description:

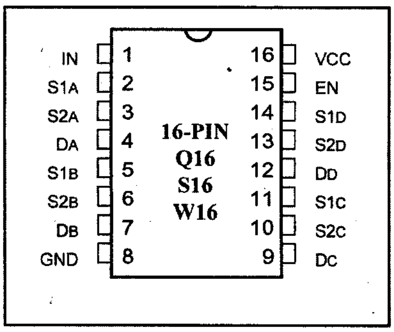
Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16-Pin Product Configuration



Product Pin Description

Pin Name	Description
S1A, S2A S1B, S2B S1C, S2C S1D, S2D	Analog Video I/O
IN	Select Input
EN	Enable
DA, DB, DC, DD	Analog Video I/O
GND	Ground
Vcc	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ±5%)

Parameters	Description	Test Conditions[1]	Min.	Typ[2]	Max.	Units
V_{ANALOG}	Analog Signal Range		0	—	2.0	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	–0.5	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=GND	—	—	±1	µA
I_O	Analog Output Leakage Current	0≤S1, S2 or D≤V_{CC}, Switch Off	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA —	–0.7	-1.2	V	
I_{OS}	Short Circuit Current[3]	S1, S2, D=0V Vcc	100	—	—	mA
V_H	Input Hysteresis at Control Pins		—	150	—	mV
R_{ON}	Switch On Resistance[4]	V_{CC}=Min., V_{IN}=1.0V R_L=75ohm, I_{ON}=13 mA	—	3	7	ohm
		V_{CC}=MIN., V_{IN}=2.0V R_L=75ohm, I_{ON}=26 mA	—	7	10	ohm

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Measured by the voltage drop between S1, S2, and D I/O pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the S1, S2, and D I/O pins.

Dynamic Characteristics (Over the Operating Range, $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 5\%$)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn On Time	R_L = 75ohm, C_L = 20 pF, see Fig. 6	—	2.5	5	ns
t_{OFF}	Turn Off Time	R_L = 75ohm, C_L = 20 pF, see Fig. 6	—	1.1	5	ns
B_W[1]	–3 dB Bandwidth	R_L = 150ohm, see Fig. 7	180	—	—	MHz
X_{TALK}	Crosstalk	R_{IN} = 10ohm; R_L = 150ohm, 10 MHz, see Fig. 7	—	–58	—	dB
D_G	Differential Gain	R_L = 150ohm, f = 3.58 MHz, see Fig. 5	—	0.64	—	%
D_P	Differential Phase	R_L = 150ohm, f = 3.58 MHz, see Fig. 5	—	0.27	—	Deg.
C_{IN}[1]	Input/Enable Capacitance	V_{IN} = 0V, f = 1 MHz	—	—	6	pF
C_{OFF}[1]	Capacitance, Switch Off	V_{IN} = 0V, f = 1 MHz	—	—	6	pF
C_{ON}[1]	Capacitance, Switch On	V_{IN} = 0V, f = 1 MHz	—	—	8	pF
O_{IRR}	Off Isolation	R_L = 150ohm, 10 MHz, see Fig. 7	—	–38	—	dB

Notes:
1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	Vcc = Max.	IN = GND or Vcc	—	0.1	3.0	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	Vcc = Max.	IN = 3.4V[3]	—	—	2.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	Vcc = Max., S1, S2, and D Pins Open $\overline{EN}$ = GND Control Input Toggling 50% Duty Cycle		—	—	0.25	mA/MHz

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); S1, S2, and D pins do not contribute to Icc.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The S1, S2, and D I/O pins generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

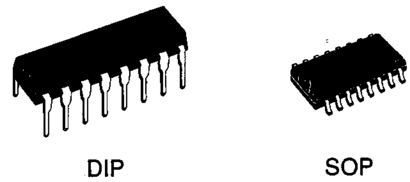
Definitions:

Symbol	Description
R_{ON}	Resistance between source and drain with switch in the ON state.
I_O	Output leakage current measured at S1, S2, and D with the switch OFF.
V_{IN}	Digital voltage at the IN pin that selects between S1 and S2 analog inputs.
V_{EN}	A voltage that ENABLES the chip.
C_{IN}	Capacitance at the digital inputs.
C_{OFF}	Capacitance at analog I/O (S1, S2, D) with switch OFF.
C_{ON}	Capacitance at analog I/O (S1, S2, D) with switch ON.
V_{IH}	Minimum input voltage for logic HIGH.
V_{IL}	Minimum input voltage for logic LOW.
I_{IH} (I_{IL})	Input current of the digital input.
I_{OS}	Minimum short circuit current for S1, S2 and D.
t_{ON}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned ON. The peak analog voltage is 0.714V.
t_{OFF}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned OFF. The peak analog voltage is 0.714V.
B_W	Frequency response of the switch in the ON state measured at 3dB down.
X_{TALK}	Is an unwanted signal coupled from channel to channel. Measured in –dB. X_{TALK} = 20 LOG V_{OUT}/V_{IN}. This is non-adjacent crosstalk.
D_G	Differential gain is the difference measurement between two bias levels, for instance analog input signals of 0V to 0.714V.
D_P	Differential phase is the difference measurement between two bias levels, for instance analog input signals of 0V to 0.714V.
O_{IRR}	Off isolation is the resistance (measured in –dB) between the input and output with the switch off (NO).

HCF4052B

Different 4-Channel Analog Multiplexer/Demultiplexer

- LOW "ON" RESISTANCE : 125Ω (Typ.) OVER 15V p.p SIGNAL-INPUT RANGE FOR V_{DD} - V_{EE} = 15V
- HIGH "OFF" RESISTANCE : CHANNEL LEAKAGE ± 100pA (Typ.) at V_{DD} - V_{EE} = 18V
- BINARY ADDRESS DECODING ON CHIP
- HIGH DEGREE OF LINEARITY : < 0.5% DISTORTION TYP. at f_{IS} = 1KHz, V_{IS} = 5 V_{pp}, V_{DD} - V_{SS} ≥ 10V, RL = 10KΩ
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS : 0.2 µW (Typ.) at V_{DD} - V_{SS} = V_{DD} - V_{EE} =10V
- MATCHED SWITCH CHARACTERISTICS : R_{ON} = 5Ω (Typ.) FOR V_{DD} - V_{EE} = 15V
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS : DIGITAL 3 to 20, ANALOG TO 20V p.p.
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



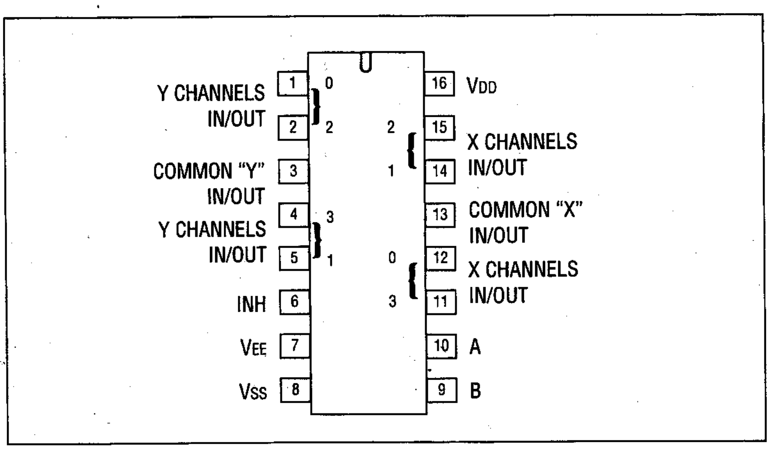
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4052BEY	
SOP	HCF4052BM1	HCF4052M013TR

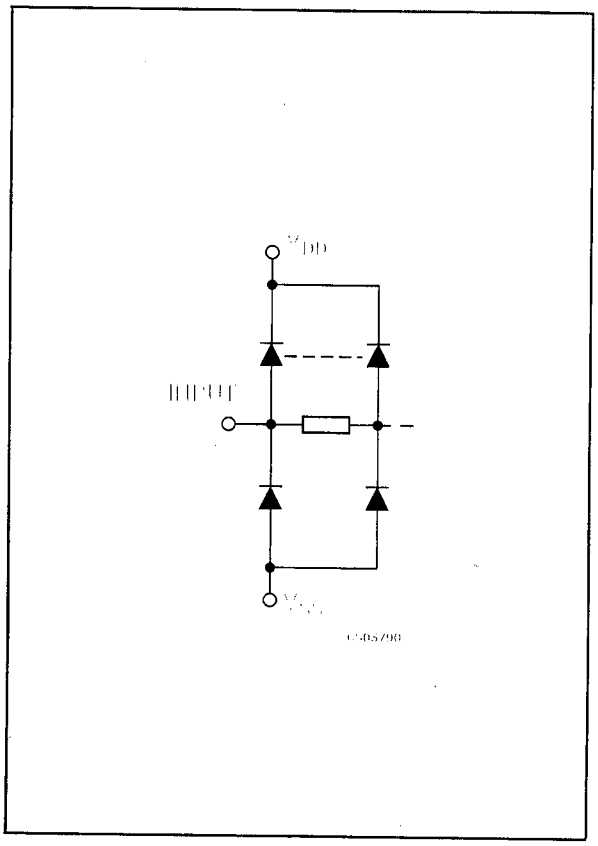
DESCRIPTION

The HCF4052B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4052B analog multiplexer/demultiplexer is a digitally controlled analog switch having low ON impedance and very low OFF leakage current. This multiplexer circuit dissipate extremely low quiescent power over the full V_{DD} - V_{SS} and V_{DD} - V_{EE} supply voltage range, independent of the logic state of the control signals.
When a logic "1" is present at the inhibit input terminal all channel are off. This device is a differential 4-channel multiplexer having two binary control inputs, A and B and an inhibit input. The two binary input signals selects 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

Pin Connection



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

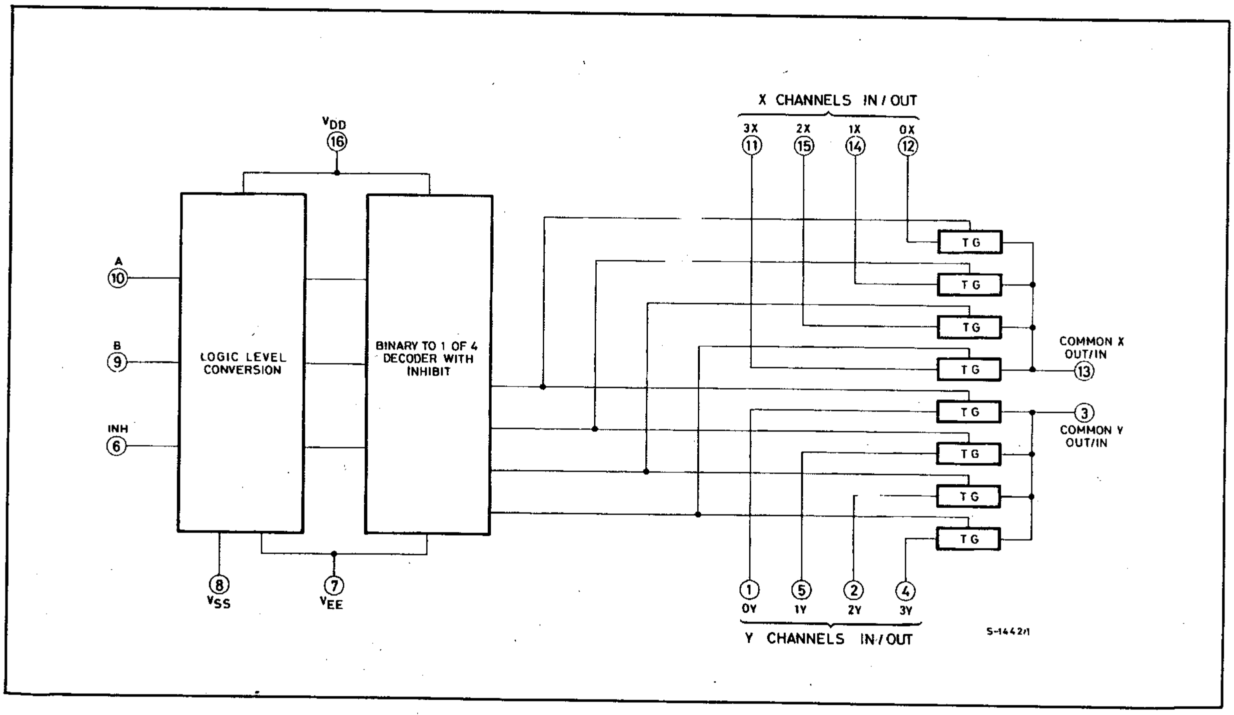
PIN No	SYMBOL	NAME AND FUNCTION
10, 9	A, B	Binary Control Inputs
6	INH	Inhibit Inputs
12, 14, 15, 11	0X to 3X CHANNEL IN/OUT	X channels Input/Output
1, 5, 2, 4	0Y to 3Y CHANNEL IN/OUT	Y channels Input/Output
3	COM Y OUT/IN	Y Common Output/Input
13	COM X OUT/IN	X Common Output/Input
7	V_{EE}	Supply Voltage
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

TRUTH TABLE

INHIBIT	B	A	
0	0	0	0x, 0y
0	0	1	1x, 1y
0	1	0	2x, 2y
0	1	1	3x, 3y
1	X	X	NONE

X : Don't Care

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	500 (*)	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

PT2259
Volume Controller IC

Description

PT2259 is an 8 -pin 2-channel volume controller which utilizes CMOS technology and incorporates the I2C interface control. The controller features an attenuation range of 0 to -79dB, low noise output, a high degree of stereo separation and req uires only a small number of external components. PT2259 is an essential component for modern audio visual systems.

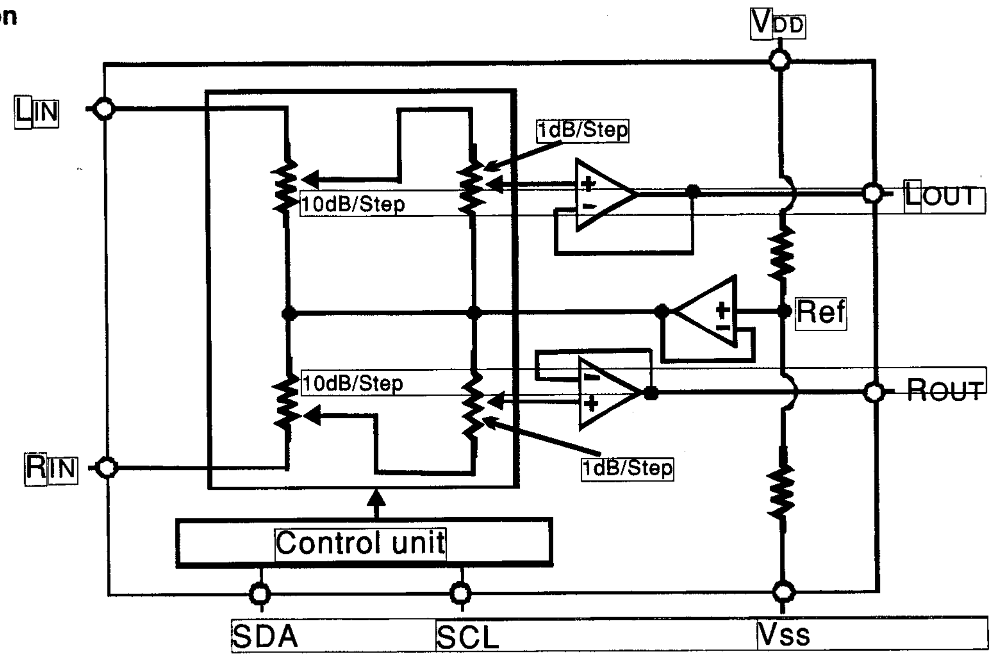
Features

- Attenuation range: 0 to –79dB in 1dB steps
- Operating voltage: 4 to 9V
- Low power consumption
- Low signal noise: S/N > 100dB (A -weighting)
- Stereo separation > 100dB
- Requires few external components
- 2-channel volume individual adjust
- DIP or SO packaging

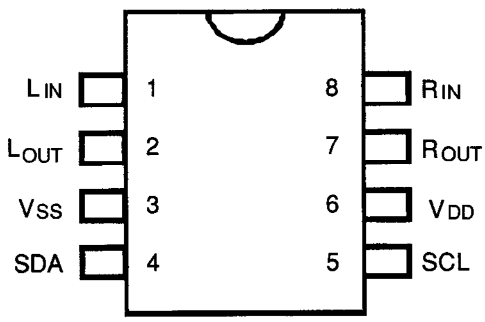
Applications

- Audio/visual surround sound systems
- Car audio systems
- Mini -compo systems
- Computer multi -media speakers
- Other audio a pplications

Pin Configuration



Pin Configuration



PT2259

Pin Description

Pin Name	I/O	Description	Pin Number
LIN	I	Left Channel Input (capacitor coupled to input port)	1
LOUT	O	Left Channel Output (capacitor coupled to output port)	2
VSS	-	Ground	3
SDA	I	I^2C Data Input	4
SCL	I	I^2C Clock Input	5
VDD	-	Power Supply	6
ROUT	O	Right Channel Output (capacitor coupled to input port)	7
RIN	I	Right Input Channel (capacitor coupled to output port)	8

CTF5510A

World Standard FST Tuner Specification

A. Measurement Conditions

1. Ambient Temperature: 25°C ± 2°C
2. Relative Humidity : 60% ±15%
3. Nominal Voltage : 5.0V ± 0.1V
4. AGC (Nominal) : 4.0V ± 0.1V
5. Tuning Voltage : 32V ± 1V
6. Input Impedance : 75Ω ± 5 Ω unbalanced
7. Output Impedance : 130Ω ± 5 Ω balanced
8. Equipment Tolerance : ≤ ± 1 dB

Note:
A proper tuner function is guaranteed within the specified supply voltage and environmental conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions. All measurements are done according to Thomson Measurements Standard for Tuners (Tocom code : 20127280) unless otherwise specified in this specification.

B. Operational Conditions

Ambient Temperature : 0°C to 60°C
Relative Humidity : 90% Max.
Tuning Supply Voltage : 32V ± 1V
B+ Supply Voltage : 5.0V ± 0.25V

C. General Data

C-1 Pin Connection

1. AGC
2. TU (N.C.)
3. AS
4. Clock (SCL)
5. Data (SDA)
6. UB (5V)
7. 5V
8. N.C.
9. VT (+32V)
10. IF_2 (balanced)
11. IF_1 (balanced)

(See mechanical drawing)

C-2 Electrical Function Range

Pin	Vcc	Impedance / Current	Ripple Voltage*
1 - AGC	0.3V to 4.0V	≥ 1 MΩ	--
4 - SCL	I^2C Bus Specifications	--	--
5 - SDA	I^2C Bus Specifications	--	--
6 - UB (+5.0V)	5.0V ± 0.25V	≤ 85 mA	≤ 5mV
9 - +32.0V	32.0V ± 1.0V	≤ 1.5 mA	≤ 5mV
10/11 - IF_2/IF_1	--	≈ 130Ω	--

* The ripple voltage must be achieved in the complete set to avoid visible interference in the video.

LM1086 -LD1086

1.5A Low Dropout Positive Regulators

General Description

The LM1086 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 1.5A of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1086 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in six fixed voltages: 1.8V, 2.5V, 2.85V, 3.3V, 3.45V and 5.0V. The fixed versions integrate the adjust resistors.

The LM1086 circuit includes a zener trimmed bandgap reference, current limiting and thermal shutdown.

The LM1086 series is available in TO-220, TO-263, and LLP packages. Refer to the LM1084 for the 5A version, and the LM1085 for the 3A version.

Features

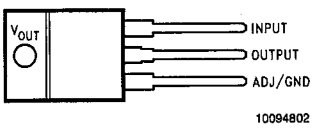
- Available in 1.8V, 2.5V, 2.85V, 3.3V, 3.45V, 5V and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 1.5A
- Line Regulation 0.015% (typical)
- Load Regulation 0.1% (typical)

Applications

- SCSI-2 Active Terminator
- High Efficiency Linear Regulators
- Battery Charger
- Post Regulation for Switching Supplies
- Constant Current Regulator
- Microprocessor Supply

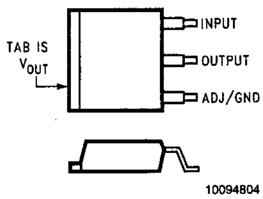
Connection Diagrams

TO-220



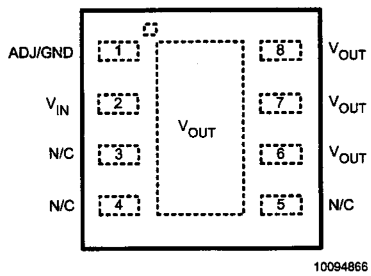
Top View

TO-263



Top View

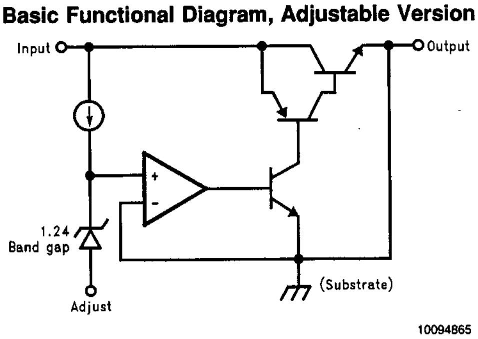
LLP



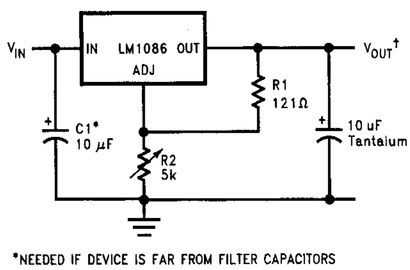
Pins 6, 7, and 8 must be tied together.

Top View

Basic Functional Diagram, Adjustable Version



Application Circuit



*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

$^{\dagger}V_{OUT} = 1.25V(1 + \frac{R2}{R1})$

10094852

1.2V to 15V Adjustable Regulator

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Maximum Input-to-Output Voltage Differential	
LM1086-ADJ	29V
LM1086-1.8	27V
LM1086-2.5	27V
LM1086-2.85	27V
LM1086-3.3	27V
LM1086-3.45	27V
LM1086-5.0	25V
Power Dissipation (Note 2)	Internally Limited
Junction Temperature (T_J)(Note 3)	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature	260°C, to 10 sec
ESD Tolerance (Note 4)	2000V

Operating Ratings (Note 1)

Junction Temperature Range (T_J) (Note 3)	
"C" Grade	
Control Section	0°C to 125°C
Output Section	0°C to 150°C
"I" Grade	
Control Section	40°C to 125°C
Output Section	40°C to 150°C

Electrical Characteristics

Typicals and limits appearing in normal type apply for T_J = 25°C. Limits appearing in Boldface type apply over the entire junction temperature range for operation.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{REF}	Reference Voltage	LM1086-ADJ I_{OUT} = 10mA, V_{IN} -V_{OUT} = 3V 10mA ≤I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5V ≤ V_{IN} - V_{OUT} ≤ 15V (Note 7)	1.238 **1.225**	1.250 **1.250**	1.262 **1.270**	V V
V_{OUT}	Output Voltage (Note 7)	LM1086-1.8 I_{OUT} = 0mA, V_{IN} = 5V 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 3.3V ≤ V_{IN} ≤ 18V	1.782 **1.764**	1.8 **1.8**	1.818 **1.836**	V
		LM1086-2.5 I_{OUT} = 0mA, V_{IN} = 5V 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 4.0V ≤ V_{IN} ≤ 18V	2.475 **2.450**	2.50 **2.50**	2.525 **2.55**	V
		LM1086-2.85 I_{OUT} = 0mA, V_{IN} = 5V 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 4.35V ≤ V_{IN} ≤ 18V	2.82 **2.79**	2.85 **2.85**	2.88 **2.91**	V V
		LM1086-3.3 I_{OUT} = 0mA, V_{IN} = 5V 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 4.75V ≤ V_{IN} ≤ 18V	3.267 **3.235**	3.300 **3.300**	3.333 **3.365**	V V
		LM1086-3.45 I_{OUT} = 0mA, V_{IN} = 5V 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 4.95V ≤ V_{IN} ≤ 18V	3.415 **3.381**	3.45 **3.45**	3.484 **3.519**	V V
		LM1086-5.0 I_{OUT} = 0mA, V_{IN} = 8V 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 6.5V ≤ V_{IN} ≤ 20V	4.950 **4.900**	5.000 **5.000**	5.050 **5.100**	V V
ΔV_{OUT}	Line Regulation (Note 8)	LM1086-ADJ I_{OUT} =10mA, 1.5V≤ (V_{IN}-V_{OUT})≤ 15V		0.015 **0.035**	0.2 **0.2**	% %
		LM1086-1.8 I_{OUT} = 0mA, 3.3V ≤ V_{IN} ≤ 18V		0.3 **0.6**	6 **6**	mV
		LM1086-2.5 I_{OUT} = 0mA, 4.0V ≤ V_{IN} ≤ 18V		0.3 **0.6**	6 **6**	mV

Electrical Characteristics (Continued)

Typicals and limits appearing in normal type apply for T_J = 25°C. Limits appearing in Boldface type apply over the entire junction temperature range for operation.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
		LM1086-2.85		0.3	6	mV
		I_{OUT} = 0mA, 4.35V ≤ V_{IN} ≤ 18V		**0.6**	**6**	mV
		LM1086-3.3		0.5	10	mV
		I_{OUT} = 0mA, 4.5V ≤ V_{IN} ≤ 18V		**1.0**	**10**	mV
		LM1086-3.45		0.5	10	mV
		I_{OUT} = 0mA, 4.95V ≤ V_{IN} ≤ 18V		**1.0**	**10**	mV
		LM1086-5.0		0.5	10	mV
		I_{OUT} = 0mA, 6.5V ≤ V_{IN} ≤ 20V		**1.0**	**10**	mV
ΔV_{OUT}	Load Regulation (Note 8)	LM1086-ADJ		0.1	0.3	%
		(V_{IN}-V_{OUT}) = 3V, 10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		**0.2**	**0.4**	%
		LM1086-1.8 ,2.5, 2.85		3	12	mV
		V_{IN} = 5V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		**6**	**20**	mV
		LM1086-3.3, 3.45		3	15	mV
		V_{IN} = 5V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		**7**	**25**	mV
		LM1086-5.0		5	20	mV
		V_{IN} = 8V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		**10**	**35**	mV
	Dropout Voltage (Note 9)	LM1086-ADJ, 1.8, 2.5,2.85, 3.3, 3.45, 5 ΔV_{REF} = 1%, I_{OUT} = 1.5A		1.3	1.5	V
I_{LIMIT}	Current Limit	LM1086-ADJ				
		V_{IN} -V_{OUT} = 5V	1.50	2.7		A
		V_{IN} -V_{OUT} = 25V	0.05	0.15		A
		LM1086-1.8,2.5, 2.85, 3.3, 3.45, V_{IN} = 8V	1.5	2.7		A
		LM1086-5.0, V_{IN} = 10V	1.5	2.7		A
	Minimum Load Current (Note 10)	LM1086-ADJ V_{IN} - V_{OUT} = 25V		5.0	10.0	mA
	Quiescent Current	LM1086-1.8, 2.5, 2.85, V_{IN} ≤ 18V		5.0	10.0	mA
		LM1086-3.3, V_{IN} ≤ 18V		5.0	10.0	mA
		LM1086-3.45, V_{IN} ≤ 18V		5.0	10.0	mA
		LM1086-5.0, V_{IN} ≤ 20V		5.0	10.0	mA
	Thermal Regulation	T_A = 25°C, 30ms Pulse		0.008	0.04	%/W
	Ripple Rejection	f_{RIPPLE} = 120Hz, C_{OUT} = 25µF Tantalum, I_{OUT} = 1.5A				
		LM1086-ADJ, C_{ADJ} = 25µF, (V_{IN} V_O) = 3V	60	75		dB
		LM1086-1.8, 2.5, 2.85, V_{IN} = 6V	60	72		dB
		LM1086-3.3, V_{IN}= 6.3V	60	72		dB
		LM1086-3.45, V_{IN}= 6.3V	60	72		dB
		LM1086-5.0 V_{IN} = 8V	60	68		dB
	Adjust Pin Current	LM1086		55	120	µA
	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5V ≤ (V_{IN}-V_{OUT})≤ 15V		0.2	5	µA
	Temperature Stability			0.5		%
	Long Term Stability	T_A = 125°C, 1000Hrs		0.3	1.0	%
	RMS Noise (% of V_{OUT})	10Hz ≤ f≤ 10kHz		0.003		%
Θ_{JC}	Thermal Resistance Junction-to-Case	3-Lead TO-263: Control Section/Output Section 3-Lead TO-220: Control Section/Output Section			1.5/4.0 1.5/4.0	°C/W °C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Power dissipation is kept in a safe range by current limiting circuitry. Refer to Overload Recovery in Application Notes. The value $_{JA}$ for the LLP package is specifically dependent on PCB trace area, trace material, and the number of thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, $_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ _{JA}$. All numbers apply for packages soldered directly into a PC board. Refer to Thermal Considerations in the Application Notes.

Note 4: For testing purposes, ESD was applied using human body model, 1.5kΩ in series with 100pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULL\ LOAD}$ Curve defines current limit as a function of input-to-output voltage. Note that 15W power dissipation for the LM1086 is only achievable over a limited range of input-to-output voltage.

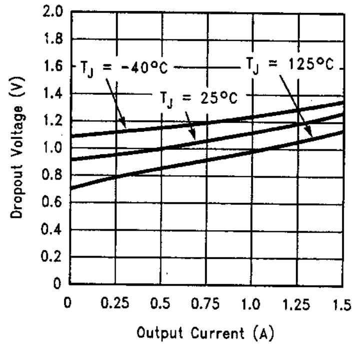
Note 8: Load and line regulation are measured at constant junction temperature, and are guaranteed up to the maximum power dissipation of 15W. Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output range.

Note 9: Dropout voltage is specified over the full output current range of the device.

Note 10: The minimum output current required to maintain regulation.

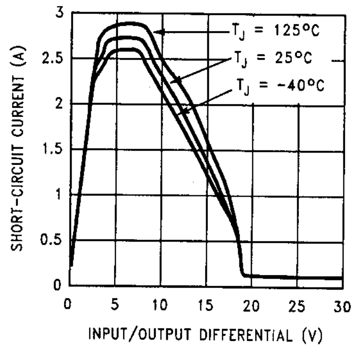
Typical Performance Characteristics

Dropout Voltage vs. Output Current



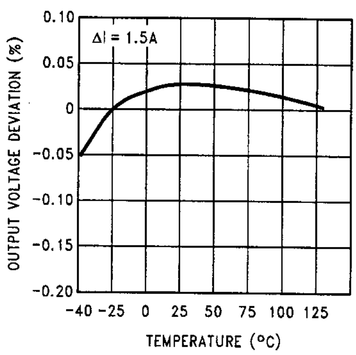
10094863

Short-Circuit Current vs. Input/Output Difference



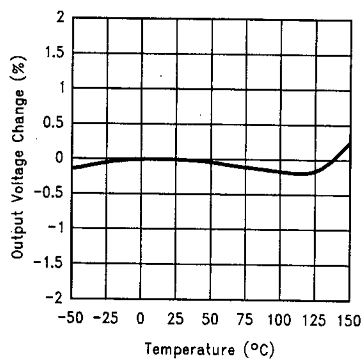
10094837

Load Regulation vs. Temperature



10094838

Percent Change in Output Voltage vs. Temperature



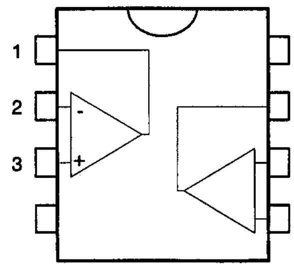
10094899

LM358
Dual Operational Amplifier

FEATURES

- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN : 100dB
- WIDE BANDWIDTH (unity gain) : 1.1MHz (temperature compen sated)
- VERY LOW SUPPLY CURRENT/OP (500mA) -ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT : 20nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE : 2mV
- LOW INPUT OFFSET CURRENT : 2nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0V TO (VCC – 1.5V)

PIN CONNECTIONS



1 - Output 1	5 - Non-inverting input 2
2 - Inverting input 1	6 - Inverting input 2
3 - Non-inverting input 1	7 - Ouput 2
4 - V_{CC}^-	8 - V_{CC}^+

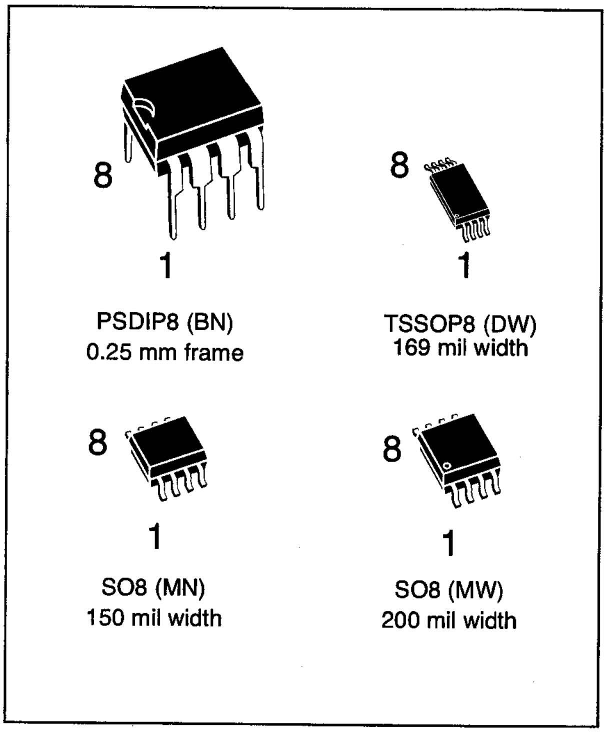
DESCRIPTION

These circuits consist of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits, which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard + 5V, which is used in logic systems and will easily, provide the required interface electronics without requiring any additional power supply. In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

M24C64

64/32 Kbit Serial I²C Bus EEPROM

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface
  Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24Cxx
  - 2.5V to 5.5V for M24Cxx-W
  - 1.8V to 3.6V for M24Cxx-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



DESCRIPTION

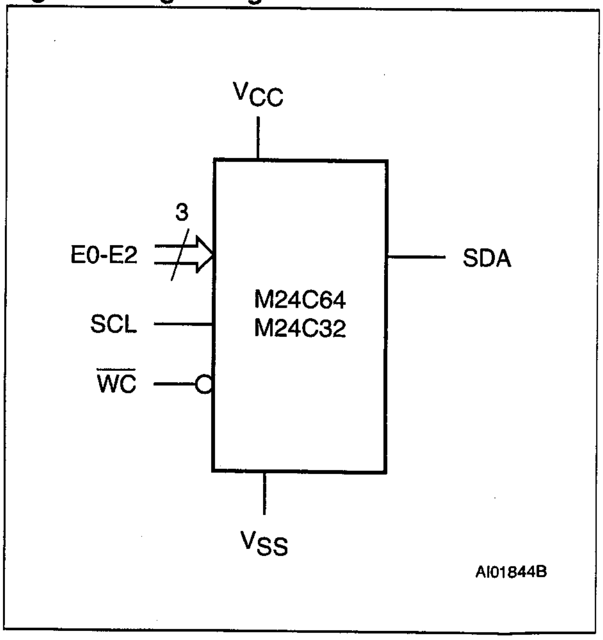
These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192x8 bits (M24C64) and 4096x8 bits (M24C32), and operate down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -R version of each device).

The M24C64 and M24C32 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



M24C64, M24C32

Figure 2A. DIP Connections

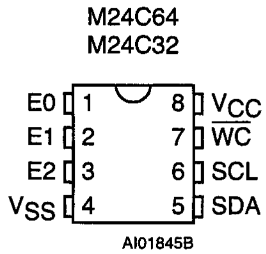
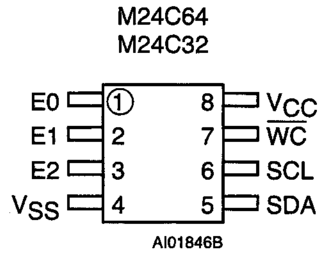


Figure 2B. SO and TSSOP Connections



These memory devices are compatible with the I²C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I²C bus definition.

The memory behaves as a slave device in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and $R\overline{W}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slow-

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 seconds SO8: 40 seconds TSSOP8: 40 seconds	260 215 215	°C
V_{IO}	Input or Output range		-0.6 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

er clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E2, E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code (but note that the V_{IL} and V_{IH} levels for the inputs are CMOS compatible, not TTL compatible).

Write Control ($\overline{WC}$)

The hardware Write Control pin ($\overline{WC}$) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ($\overline{WC}=V_{IL}$) or disable ($\overline{WC}=V_{IH}$) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}, and write operations are allowed.

When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

DEVICE OPERATION

The memory device supports the I^2C protocol. This is summarized in Figure 4, and is compared with other serial bus protocols in Application Note *AN1001*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

MC34164; MC33164

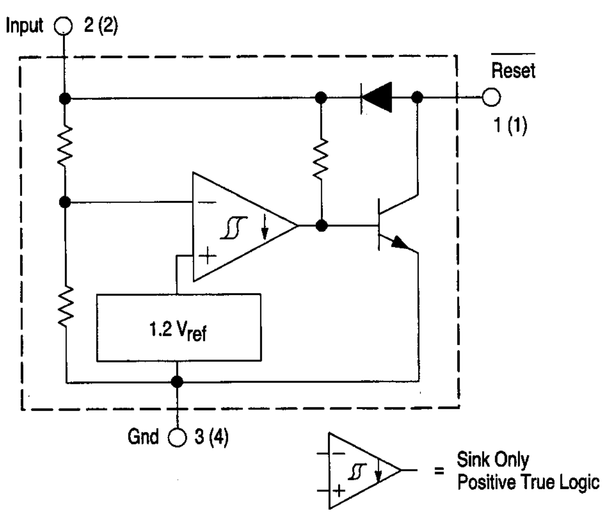
Micropower Undervoltage Sensing Circuits

The MC34164 series are undervoltage sensing circuits specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is required. These devices offer the designer an economical solution for low voltage detection with a single external resistor. The MC34164 series features a bandgap reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 6.0 mA, and guaranteed operation down to 1.0 V input with extremely low standby current. These devices are packaged in 3–pin TO–226AA, 8–pin SO–8 and Micro–8 surface mount packages.

Applications include direct monitoring of the 3.0 or 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Monitors 3.0 V (MC34164–3) or 5.0 V (MC34164–5) Power Supplies
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 6.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation With 1.0 V Input
- Extremely Low Standby Current: As Low as 9.0 µA
- Economical TO–226AA, SO–8 and Micro–8 Surface Mount Packages

Representative Block Diagram

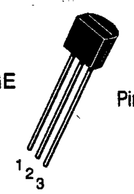


Pin numbers adjacent to terminals are for the 3–pin TO–226AA package.
Pin numbers in parenthesis are for the 8–lead packages.

This device contains 28 active transistors.

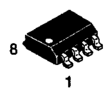
TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA)

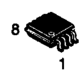


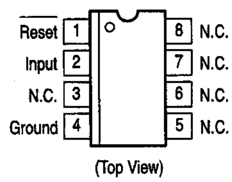
Pin 1. $\overline{\text{Reset}}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)





ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34164D–3	T_A = 0° to +70°C	SO–8
MC34164D–5		
MC34164DM–3		Micro–8
MC34164DM–5		
MC34164P–3		TO–226AA
MC34164P–5		
MC33164D–3	T_A = –40° to +125°C	SO–8
MC33164D–5		
MC33164DM–3		Micro–8
MC33164DM–5		
MC33164P–3		TO–226AA
MC33164P–5		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 12	V
Reset Output Voltage	V_O	–1.0 to 12	V
Reset Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	700	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	700	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
DM Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	520	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC34164 Series		0 to +70	
MC33164 Series		– 40 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

NOTE: ESD data available upon request.

MC34164–3, MC33164–3 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	2.55	2.71	2.80	
Low State Output (V_{in} Decreasing)	V_{IL}	2.55	2.65	2.80	
Hysteresis (I_{Sink} = 100 µA)	V_H	0.03	0.06	–	
RESET OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 2.4 V, I_{Sink} = 1.0 mA)		–	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		–	0.1	0.3	
Output Sink Current (V_{in}, Reset = 2.4 V)	I_{Sink}	6.0	12	30	mA
Output Off–State Leakage	$I_{R(leak)}$				µA
(V_{in}, Reset = 3.0 V)		–	0.02	0.5	
(V_{in}, Reset = 10 V)		–	0.02	1.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	6.0	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	–	–	V
Quiescent Input Current	I_{in}				µA
V_{in} = 3.0 V		–	9.0	15	
V_{in} = 6.0 V		–	24	40	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164 – 40°C for MC33164; T_{high} = + 70°C for MC34164 = + 85°C for MC33164

MC34164–5, MC33164–5 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.15	4.33	4.45	
Low State Output (V_{in} Decreasing)	V_{IL}	4.15	4.27	4.45	
Hysteresis (I_{Sink} = 100 µA)	V_H	0.02	0.09	–	
RESET OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 1.0 mA)		–	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		–	0.1	0.3	
Output Sink Current (V_{in}, Reset = 4.0 V)	I_{Sink}	7.0	20	50	mA
Output Off–State Leakage	$I_{R(leak)}$				µA
(V_{in}, Reset = 5.0 V)		–	0.02	0.5	
(V_{in}, Reset = 10 V)		–	0.02	2.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	–	–	V
Quiescent Input Current	I_{in}				µA
V_{in} = 5.0 V		–	12	20	
V_{in} = 10 V		–	32	50	

NOTES: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164 T_{high} = + 70°C for MC34164
– 40°C for MC33164 = + 85°C for MC33164

Figure 1. MC3X164–3 Reset Output Voltage versus Input Voltage

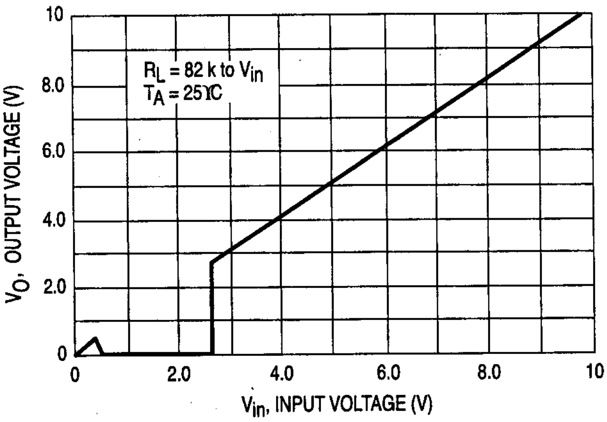


Figure 2. MC3X164–5 Reset Output Voltage versus Input Voltage

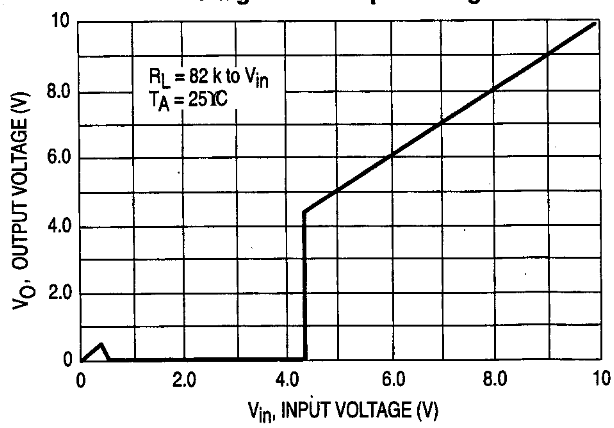


Figure 3. MC3X164–3 Reset Output Voltage versus Input Voltage

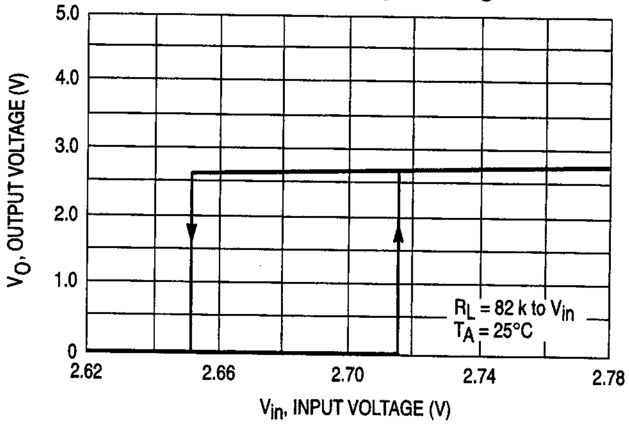


Figure 4. MC3X164–5 Reset Output Voltage versus Input Voltage

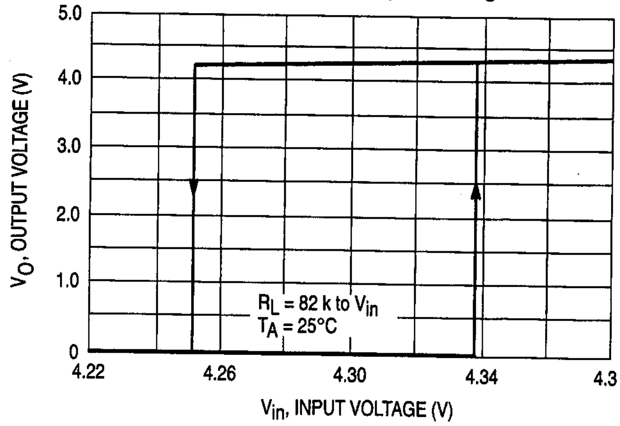


Figure 5. MC3X164–3 Comparator Threshold Voltage versus Temperature

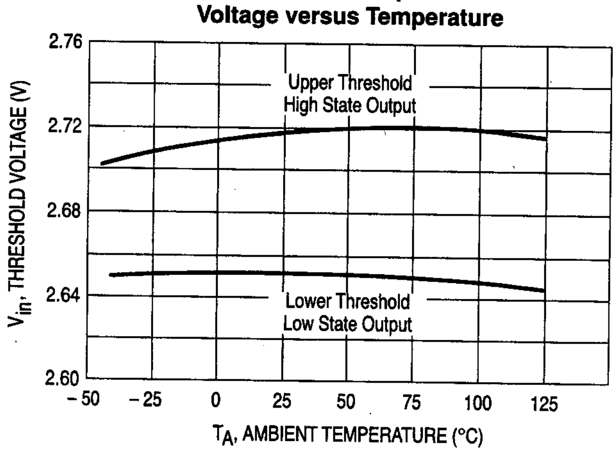


Figure 6. MC3X164–5 Comparator Threshold Voltage versus Temperature

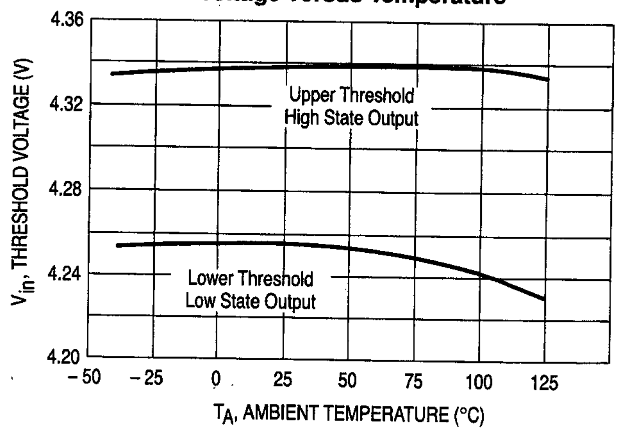


Figure 7. MC3X164–3 Input Current versus Input Voltage

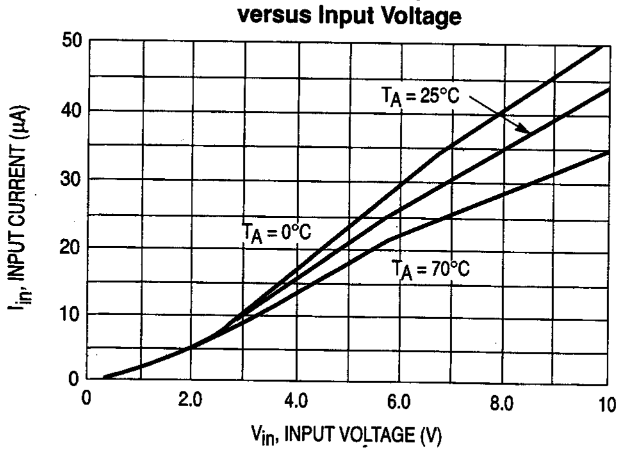


Figure 8. MC3X164–5 Input Current versus Input Voltage

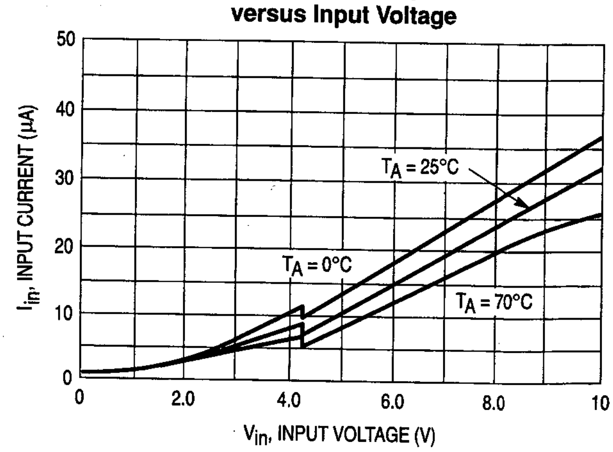


Figure 9. MC3X164–3 Reset Output Saturation versus Sink Current

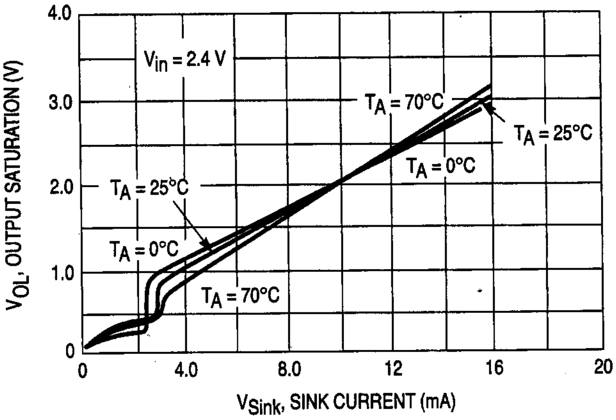


Figure 10. MC3X164–5 Reset Output Saturation versus Sink Current

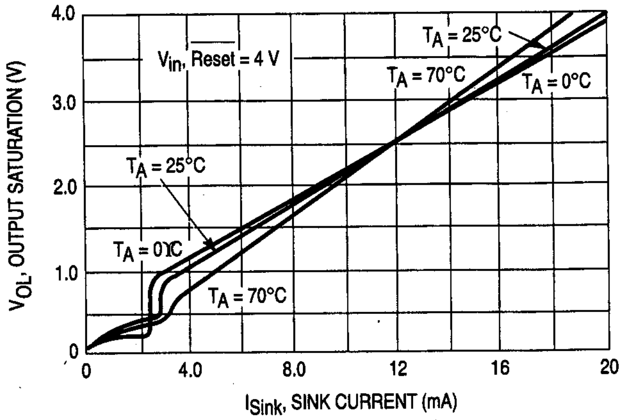


Figure 11. Clamp Diode Forward Current versus Voltage

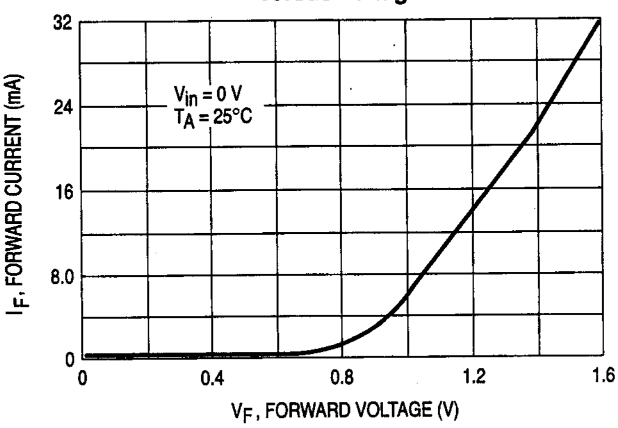


Figure 12. $\overline{\text{Reset}}$ Delay Time (MC3X164–5 Shown)

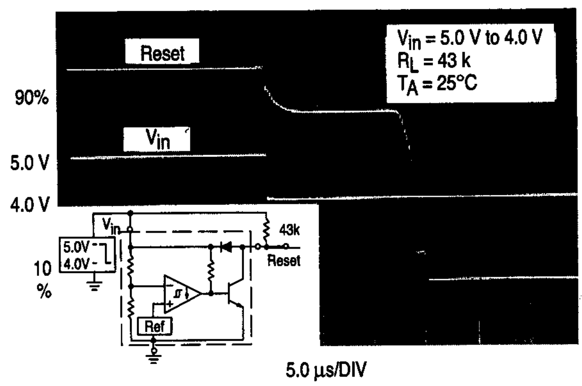
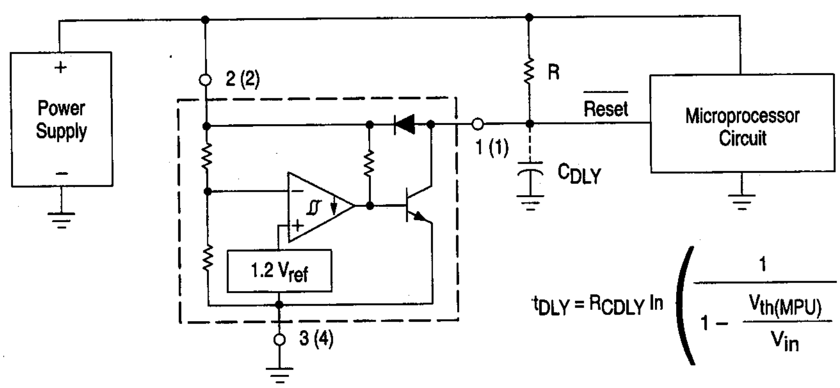


Figure 13. Low Voltage Microprocessor Reset



$$t_{DLY} = R_{CDLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}} \right)$$

A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (< 500 ns) it is recommended that the RCDLY time constant be greater than 5.0 μs. $V_{th(MPU)}$ is the microprocessor reset input threshold.

Table 3: Parallel Input/Output Pins (page 3 of 3)

Pin No.	Pin Name	Main Function (after Reset)	Alternate Function	POR Value	If not used
7	PORTD2	Port D2	Timer Input 2 / Timer Output 3/Vsync Input	Input	Output PP = 0, NC
8	PORTD3	Port D3	Timer Input 3 / Timer Output 2	Input	Output PP = 0, NC
132	PORTD4	Port D4	IR_in	Input	Output PP = 0, NC
147	PORTD5	Port D5	GFX_ACTIVE used for VGA or external up-converter	Input	Output PP = 0, NC
9	PORTD6	Port D6	INT0	Input	Output PP = 0, NC
134	PORTD7	Port D7	INT1/16xUART Clock	Input	Output PP = 0, NC

Table 4: External Memory Interface Pins (page 1 of 3)

Pin No.	Pin Name	Pin Description	POR Value	If not used
Flash Data Bus				
90	FLASH_D0	Flash Data Bus 0	Input	n/a
88	FLASH_D1	Flash Data Bus 1	Input	n/a
86	FLASH_D2	Flash Data Bus 2	Input	n/a
84	FLASH_D3	Flash Data Bus 3	Input	n/a
80	FLASH_D4	Flash Data Bus 4	Input	n/a
78	FLASH_D5	Flash Data Bus 5	Input	n/a
76	FLASH_D6	Flash Data Bus 6	Input	n/a
74	FLASH_D7	Flash Data Bus 7	Input	n/a
89	FLASH_D8	Flash Data Bus 8	Input	n/a
87	FLASH_D9	Flash Data Bus 9	Input	n/a
85	FLASH_D10	Flash Data Bus 10	Input	n/a
83	FLASH_D11	Flash Data Bus 11	Input	n/a
79	FLASH_D12	Flash Data Bus 12	Input	n/a
77	FLASH_D13	Flash Data Bus 13	Input	n/a
75	FLASH_D14	Flash Data Bus 14	Input	n/a
73	FLASH_D15	Flash Data Bus 15	Input	n/a
SDRAM Data Bus				
23	SDRAM_D0	SDRAM Data Bus 0	Input	n/a
22	SDRAM_D1	SDRAM Data Bus 1	Input	n/a
21	SDRAM_D2	SDRAM Data Bus 2	Input	n/a

MCR22-6; MCR22-8

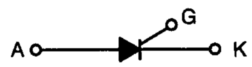
Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed and tested for repetitive peak operation required for CD ignition, fuel ignitors, flash circuits, motor controls and low-power switching applications.

- 150 Amperes for 2 μs Safe Area
- High dv/dt
- Very Low Forward "On" Voltage at High Current
- Low-Cost TO-226AA (TO-92)
- Device Marking: Device Type, e.g., MCR22–6, Date Code

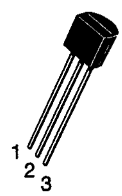
SCRs
1.5 AMPERES RMS
400 thru 600 VOLTS



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage (R_{GK} = IK, T_J = -40 to +110°C, Sine Wave, 50 to 60 Hz, Gate Open) MCR22–6 MCR22–8	V_{DRM}, V_{RRM}	400 600	Volts
On-State Current RMS (180° Conduction Angles, T_C = 80°C)	$I_{T(RMS)}$	1.5	Amps
Peak Non-repetitive Surge Current, T_A = 25°C (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	15	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.9	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_A = 25°C)	P_{GM}	0.5	Watt
Forward Average Gate Power (t = 8.3 msec, T_A = 25°C)	$P_{G(AV)}$	0.1	Watt
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, T_A = 25°C)	I_{FGM}	0.2	Amp
Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μs, T_A = 25°C)	V_{RGM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	–40 to +110	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



TO–92 (TO–226AA)
CASE 029
STYLE 10

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	160	°C/W
Lead Solder Temperature (Lead Length ≥1/16 from case, 10 s Max)	T_L	+260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

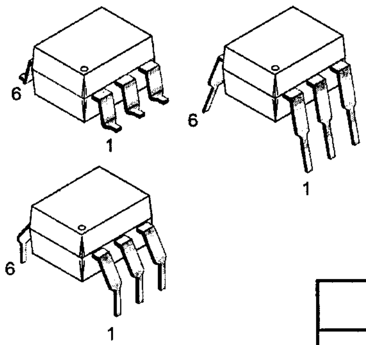
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}; R_{GK} = 1000 Ohms)	T_C = 25°C T_C = 110°C	I_{DRM}, I_{RRM}	– –	– –	10 200	μA μA
ON CHARACTERISTICS						
Peak Forward On–State Voltage(1) (I_{TM} = 1 A Peak)		V_{TM}	–	1.2	1.7	Volts
Gate Trigger Current (Continuous dc)(2) (V_{AK} = 6 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = –40°C	I_{GT}	– –	30 –	200 500	μA
Gate Trigger Voltage (Continuous dc)(2) (V_{AK} = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = –40°C	V_{GT}	– –	– –	0.8 1.2	Volts
Gate Non–Trigger Voltage(1) (V_{AK} = 12 Vdc, R_L = 100 Ohms)	T_C = 110°C	V_{GD}	0.1	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, Gate Open) Initiating Current = 200 mA	T_C = 25°C T_C = –40°C	I_H	– –	2.0 –	5.0 10	mA
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off–State Voltage (T_C = 110°C)		dv/dt	–	25	–	V/μs

(1) Pulse Width = 1.0 ms, Duty Cycle ≤1%.
(2) R_{GK} Current not included in measurement.

MOC3031M; MOC3032M; MOC3033M; MOC3041M
MOC 3042M; MOC 3043M
6-Pin Dip Zero-Cross Optoisolators Triac Driver Output

DESCRIPTION
The MOC303XM and MOC304XM devices consist of a AlGaAs infrared emitting diode optically coupled to a monolithic silicon detector performing the function of a zero voltage crossing bilateral triac driver.

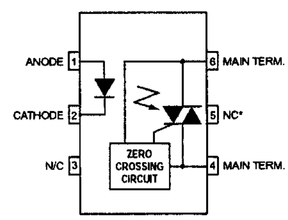
They are designed for use with a triac in the interface of logic systems to equipment powered from 115 VAC lines, such as teletypewriters, CRTs, solid-state relays, industrial controls, printers, motors, solenoids and consumer appliances, etc.



FEATURES
- Simplifies logic control of 115 VAC power
- Zero voltage crossing
- dv/dt of 2000 V/µs typical, 1000 V/µs guaranteed
- VDE recognized (File # 94766)
  -ordering option V (e.g., MOC3043VM)

APPLICATIONS
- Solenoid/valve controls
- Static power switches
- Temperature controls
- AC motor starters
- Lighting controls
- AC motor drives
- E.M. contactors
- Solid state relays

SCHEMATIC



*DO NOT CONNECT (TRIAC SUBSTRATE)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameters	Symbol	Device	Value	Units
TOTAL DEVICE Storage Temperature	T_{STG}	All	-40 to +150	°C
Operating Temperature	T_{OPR}	All	-40 to +85	°C
Lead Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
Junction Temperature Range	T_J	All	-40 to +100	°C
Isolation Surge Voltage(1) (peak AC voltage, 60Hz, 1 sec duration)	V_{ISO}	All	7500	Vac(pk)
Total Device Power Dissipation @ 25°C	P_D	All	250	mW
Derate above 25°C			2.94	mW/°C
EMITTER Continuous Forward Current	I_F	All	60	mA
Reverse Voltage	V_R	All	6	V
Total Power Dissipation 25°C Ambient	P_D	All	120	mW
Derate above 25°C			1.41	mW/°C
DETECTOR Off-State Output Terminal Voltage	V_{DRM}	MOC3031M/2M/3M	250	V
		MOC3041M/2M/3M	400	
Peak Repetitive Surge Current (PW = 100 µs, 120 pps)	I_{TSM}	All	1	A
Total Power Dissipation @ 25°C Ambient	P_D	All	150	mW
Derate above 25°C		All	1.76	mW/°C

Note
1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
EMITTER							
Input Forward Voltage	I_F = 30 mA	V_F	All		1.25	1.5	V
Reverse Leakage Current	V_R = 6 V	I_R	All		0.01	100	µA
DETECTOR							
Peak Blocking Current,Either Direction	Rated V_{DRM}, I_F = 0 (note 1)	I_{DRM1}	All			100	nA
Peak On-State Voltage,Either Direction	I_{TM} = 100 mA peak, I_F = 0	V_{TM}	All		1.8	3	V
Critical Rate of Rise of Off-State Voltage	I_F = 0 (figure 9, note 3)	dv/dt	All	1000			V/µs

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
LED Trigger Current	Main terminal voltage = 3V (note 2)	I_{FT}	MOC3031M/MOC3041M			15	mA
			MOC3032M/MOC3042M			10	
			MOC3033M/MOC3043M			5	
Holding Current, Either Direction		I_H	All		400		µA

ZERO CROSSING CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
Inhibit Voltage	I_F = rated I_{FT}, MT1-MT2 voltage above which device will not trigger off-state	V_{IH}	All			20	V
Leakage in Inhibited State	I_F = rated I_F, rated V_{DRM}, off-state	I_{DRM2}	All			500	µA

Note

1. Test voltage must be applied within dv/dt rating.
2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3031M & MOC3041M, 10 mA for MOC3032M & MOC3042M, 5 mA for MOC3033M & MOC3043M) and absolute max I_F (60 mA).
3. This is static dv/dt. See Figure 9 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

74AHC1G08; 74AHCT1G08

2-input AND gate

FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Low power dissipation
- Balanced propagation delays
- Very small 5-pin package
- Output capability: standard
- Specified from −40 to +125 °C.

DESCRIPTION

The 74AHC1G/AHCT1G08 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G08 provides the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC1G	AHCT1G	
t_{PHL}/t_{PLH}	propagation delay A and B to Y	C_L = 15 pF; V_{CC} = 5 V	3.2	3.6	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	17	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUTS		OUTPUT
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC1G08GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	AE
74AHCT1G08GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	CE
74AHC1G08GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	A08
74AHCT1G08GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	C08

PINNING

PIN	SYMBOL	DESCRIPTION
1	B	data input B
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

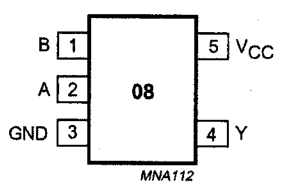


Fig.1 Pin configuration.

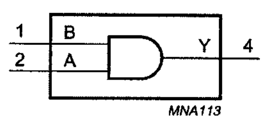


Fig.2 Logic symbol.

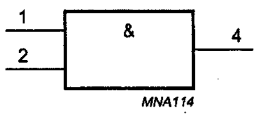


Fig.3 IEC logic symbol.

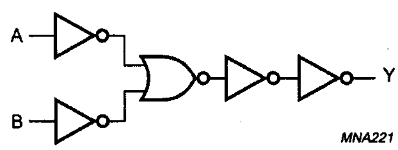


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC1G			74AHCT1G			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall times	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V	–	–20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V	–	±25	mA
I_{CC}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C	–	250	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

BU4525AX

Silicon Diffused Power Transistor

GENERAL DESCRIPTION

Enhanced performance, new generation, high voltage, high-speed switching npn transistor in a plastic full-pack envelope intended for use in horizontal deflection circuits of colour television receivers and p.c. monitors. Featuresexceptional tolerance to base drive and collector current load variations resulting in a very low worst case dissipation.

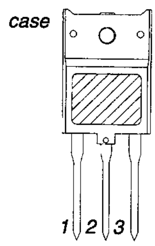
QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	$V_{BE} = 0V$	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	800	V
I_C	collector current (DC)		–	12	A
I_{CM}	collector current peak value		–	30	A
P_{tot}	total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
V_{CEsat}	collector - emitter saturation voltage	$I_C = 9$ A; $I_B = 2.25$ A	–	3.0	V
I_{Csat}	collector saturation current	f = 16kHz	9.0	–	A
		f = 70kHz	7.0	–	A
t_f	fall time	$I_{csat} = 9.0$ A; f = 16kHz	0.4	0.55	µs
		$I_{csat} = 7.0$ A; f = 70kHz	0.15	–	µs

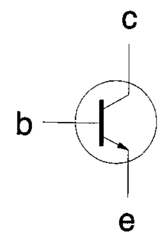
PINNING - SOT399

Pin	Description
1	base
2	collector
3	emitter
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	$V_{BE} = 0V$	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	800	V
I_C	collector current (DC)		–	12	A
I_{CM}	collector current peak value		–	30	A
I_B	Base current (DC)		–	8	A
I_{BM}	Base current peak value		–	12	mA
$-I_{BM}$	Reverse base current peak value[1]		–	7	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		–	150	°C

THERMAL RESISTANCES

Symbol	Parameter	Conditions	Typ.	Max.	Unit
$R_{th\ j\text{-}hs}$	Junction to heatsink	with heatsink compound	–	2.8	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	35	–	K/W

1 Turn-off current.

ISOLATION LIMITING VALUE & CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H.≤ 65%; clean and dustfree	–		2500	V
C_{isol}	Capaticance from T2 to external heatsink	f= 1 MHz	–	22	–	pF

STATIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{ces}	Collector cut-off current [2]	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	–	–	1.0	mA
I_{ces}		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$[2] T_j = 125 °C	–	–	2.0	mA
I_{EBO}	Emitter cut-off current	V_{EB} = 6.0 V; I_C = 0A	–	–	100	µA
BV_{EBO}	Emitter -base breakdown voltage	I_B =1 mA	7.5	13.5	–	V
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0A; I_c = 100 mA; L = 25 mH	800	–	–	V
V_{CEsat}	Collector-emitter saturation voltages	I_C = 9.0 A; I_B = 2.25 A	–	–	3.0	V
V_{BEsat}	Base-emitter saturation voltages	I_C = 9.0 A; I_B = 2.25 A	0.88	0.97	1.06	V
h_{FE}	DC current gain	I_C = 1.0A; V_{CE} = 5 V	–	12	–	
		I_C = 9.0 A; V_{CE} = 5 V	4.2	5.8	7.6	

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_c	Collector capacitance	I_E = 0A; V_{CB} = 10V; f = 1 MHz	145	–	pF
	Switching times (16 kHz line deflection circuit)	I_{Csat} = 9.0 A;I_{B1}= 1.8 A (I_{B2}=-4.5 A)			
t_s	Turn-off storage time		3.7	4.5	µs
t_f	Turn-off fall time		0.4	0.55	µs
	Switching times (70 kHz line deflection circuit)	I_{Csat} = 7.0 A;I_{B1}= 1.4 A (I_{B2}=-4.5 A)			
t_s	Turn-off storage time		2	–	µs
t_f	Turn-off fall time		0.15	–	µs

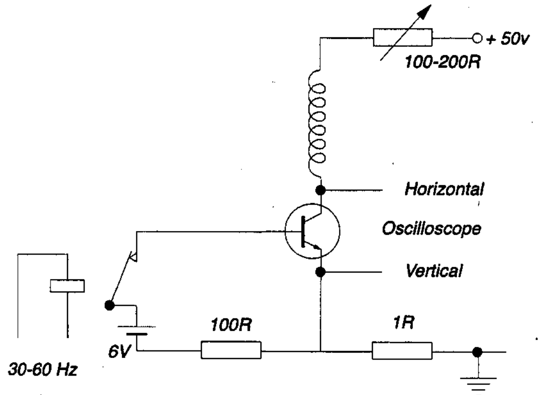


Fig.1. Test circuit for $V_{CEOsust}$.

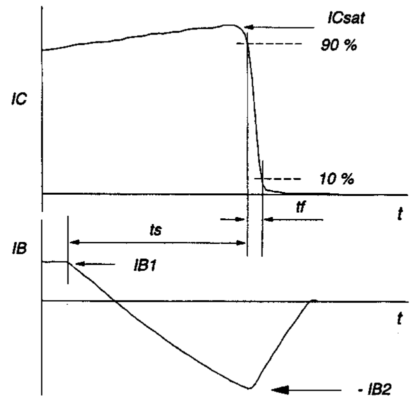


Fig.4. Switching times definitions.

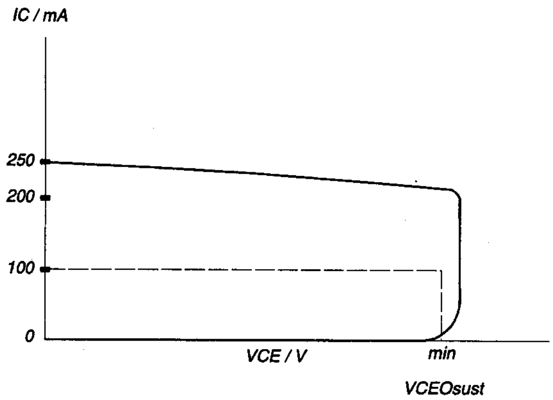


Fig.2. Oscilloscope display for $V_{CEOsust}$.

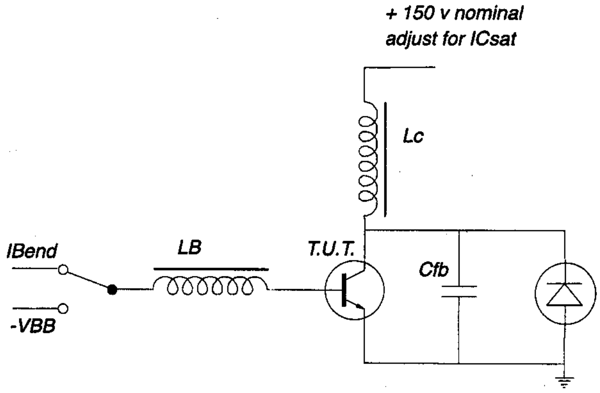


Fig.5. Switching times test circuit.

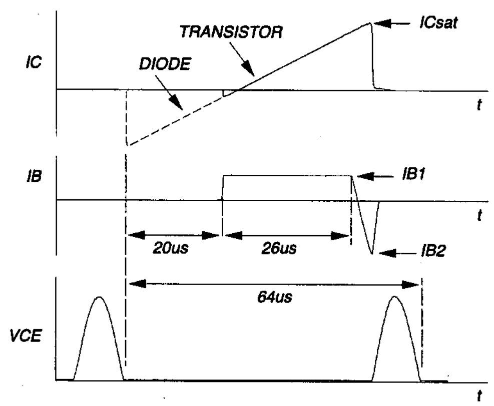


Fig.3. Switching times waveforms (16 kHz).

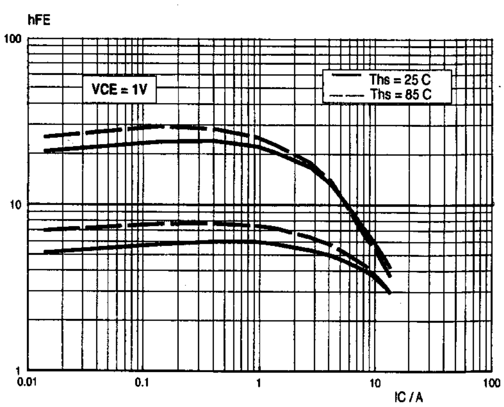


Fig.6. High and low DC current gain.

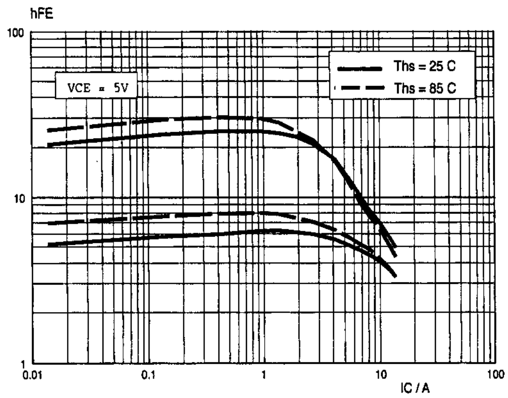


Fig.7. High and low DC current gain.

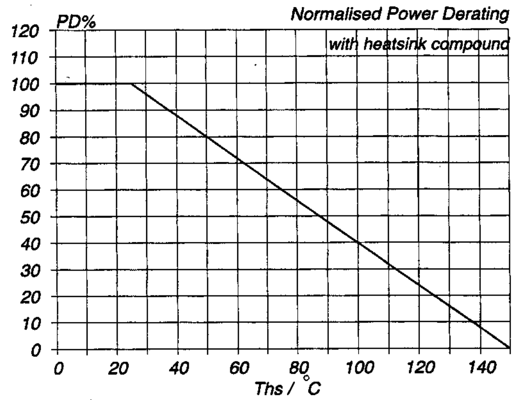


Fig.10. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\,25°C}$

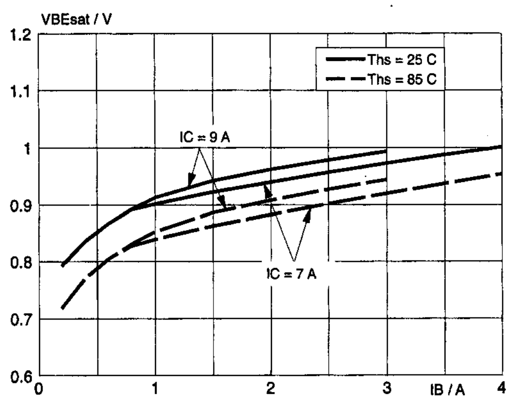


Fig.8. Typical base-emitter saturation voltage.

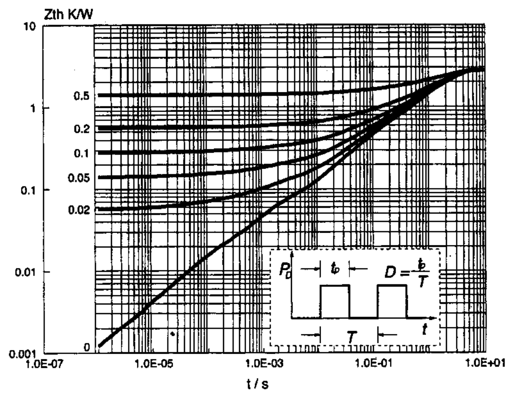


Fig.11. Transient thermal impedance.

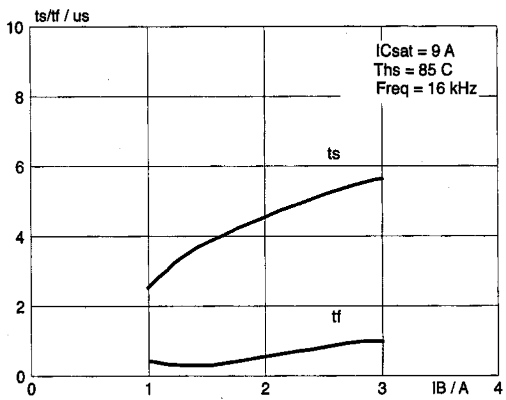


Fig.9. Typical collector storage and fall time.
$I_C = 9\,A$; $T_j = 85°C$; $f = 16kHz$

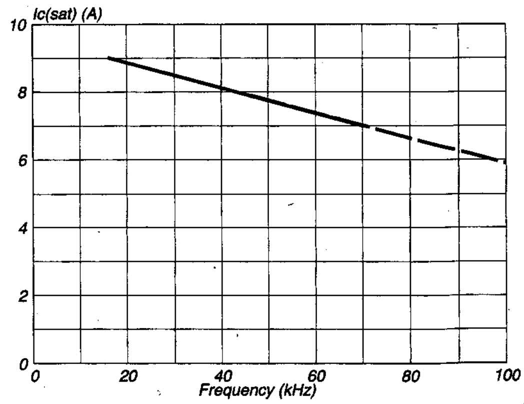
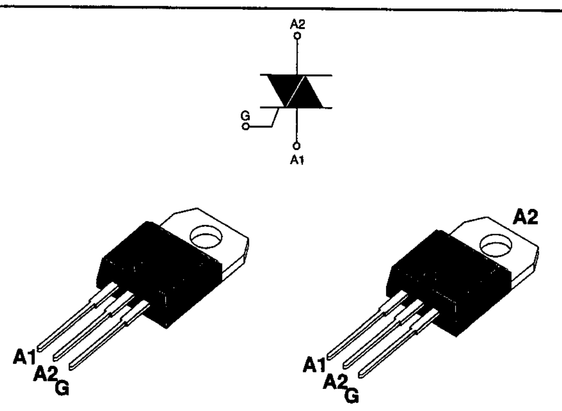


Fig.12. I_{Csat} during normal running vs. frequency of operation for optimum performance

BTA/BTB06 series
6A Triacs

MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	6	A
V_{DRM}/V_{RRM}	600 and 800	V
$I_{G\,(Q_1)}$	5 to 50	mA



TO-220AB Insulated (BTA06)

TO-220AB (BTB06)

DESCRIPTION

Suitable for AC switching operations, the BTA/BTB06 series can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control in light dimmers, motor speed controllers,...

The snubberless and logic level versions (BTA/BTB...W) are specially recommended for use on inductive loads, thanks to their high commutation performances. By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at 2500V RMS) complying with UL standards (File ref.: E81734)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TO-220AB	Tc = 110°C	6	A
		TO-220AB Ins.	Tc = 105°C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, Tj initial = 25°C)	F = 50 Hz	t = 20 ms	60	A
		F = 60 Hz	t = 16.7 ms	63	
I^2t	I^2t Value for fusing	tp = 10 ms		21	A^2s
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, tr ≤ 100 ns	F = 120 Hz	Tj = 125°C	50	A/μs
I_{GM}	Peak gate current	tp = 20 μs	Tj = 125°C	4	A
$P_{G(AV)}$	Average gate power dissipation		Tj = 125°C	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	°C

BTA/BTB06 Series

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise specified)

■ SNUBBERLESS™ and LOGIC LEVEL (3 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB06 TW	SW	CW	BW	Unit
I_{GT} (1)	$V_D = 12$ V $R_L = 30\ \Omega$	I - II - III	MAX.	5	10	35	50	mA
V_{GT}		I - II - III	MAX.	1.3				V
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3$ kΩ Tj = 125°C	I - II - III	MIN.	0.2				V
I_H (2)	$I_T = 100$ mA		MAX.	10	15	35	50	mA
I_L	$I_G = 1.2\ I_{GT}$	I - III	MAX.	10	25	50	70	mA
		II		15	30	60	80	
dV/dt (2)	$V_D =$ 67 %V_{DRM} gate open Tj = 125°C		MIN.	20	40	400	1000	V/µs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs Tj = 125°C		MIN.	2.7	3.5	-	-	A/ms
	(dV/dt)c = 10 V/µs Tj = 125°C			1.2	2.4	-	-	
	Without snubber Tj = 125°C			-	-	3.5	5.3	

■ STANDARD (4 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB06 C	B	Unit
I_G (1)	$V_D = 12$ V $R_L = 30\ \Omega$	I - II - III IV	MAX.	25 50	50 100	mA
V_{GT}		ALL	MAX.	1.3		V
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3$ kΩ Tj = 125°C	ALL	MIN.	0.2		V
I_H (2)	$I_T = 500$ mA		MAX.	25	50	mA
I_L	$I_G = 1.2\ I_{GT}$	I - III - IV	MAX.	40	50	mA
		II		80	100	
dV/dt (2)	$V_D =$ 67 %V_{DRM} gate open Tj = 125°C		MIN.	200	400	V/µs
(dV/dt)c (2)	(dI/dt)c = 2.7 A/ms Tj = 125°C		MIN.	5	10	V/µs

STATIC CHARACTERISTICS

Symbol	Test Conditions			Value	Unit
V_T (2)	$I_{TM} = 5.5$ A tp = 380 µs	Tj = 25°C	MAX.	1.55	V
V_{to} (2)	Threshold voltage	Tj = 125°C	MAX.	0.85	V
R_d (2)	Dynamic resistance	Tj = 125°C	MAX.	60	mΩ
I_{DRM}	$V_{DRM} = V_{RRM}$	Tj = 25°C	MAX.	5	µA
I_{RRM}		Tj = 125°C		1	mA

Note 1: minimum IGT is guaranted at 5% of IGT max.

Note 2: for both polarities of A2 referenced to A1

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	TO-220AB	1.8	°C/W
		TO-220AB Insulated	2.7	
$R_{th(j-a)}$	Junction to ambient	TO-220AB TO-220AB Insulated	60	°C/W

PRODUCT SELECTOR

Part Number	Voltage (xxx)		Sensitivity	Type	Package
	600 V	800 V			
BTA/BTB06-xxxB	X	X	50 mA	Standard	TO-220AB
BTA/BTB06-xxxBW	X	X	50 mA	Snubberless	TO-220AB
BTA/BTB06-xxxC	X	X	25 mA	Standard	TO-220AB
BTA/BTB06-xxxCW	X	X	35 mA	Snubberless	TO-220AB
BTA/BTB06-xxxSW	X	X	10 mA	Logic level	TO-220AB
BTA/BTB06-xxxTW	X	X	5 mA	Logic level	TO-220AB

BTB: non insulated TO-220AB package

ORDERING INFORMATION

BT A 06 - 600 BW (RG)

TRIAC SERIES

INSULATION:
A: insulated
B: non insulated

CURRENT: 6A

VOLTAGE:
600: 600V
800: 800V

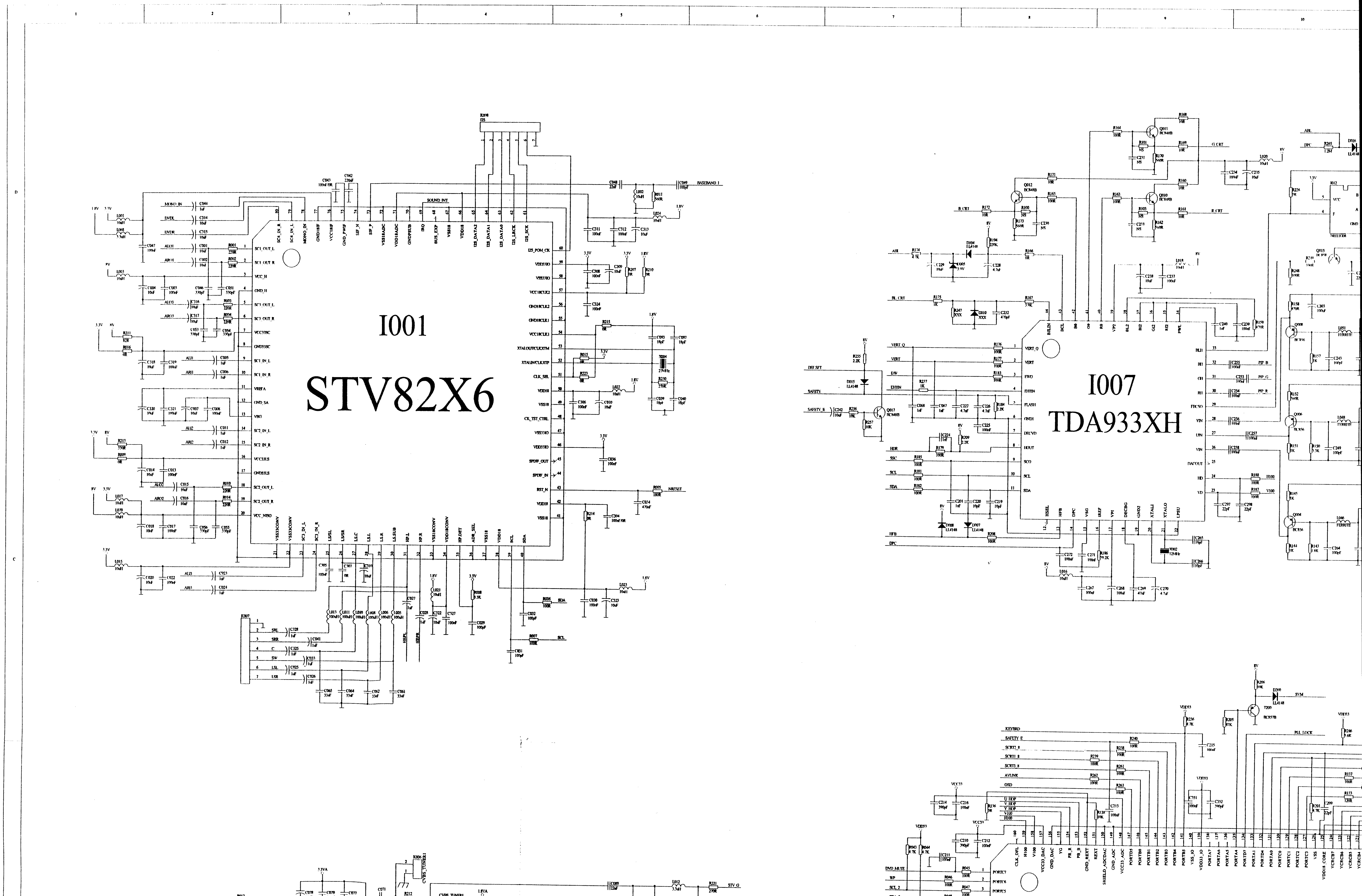
SENSITIVITY & TYPE
B: 50mA STANDARD
BW: 50mA SNUBBERLESS
C: 25mA STANDARD
CW: 35mA SNUBBERLESS
SW: 10mA LOGIC LEVEL
TW: 5mA LOGIC LEVEL

PACKING MODE
Blank: Bulk
RG: Tube

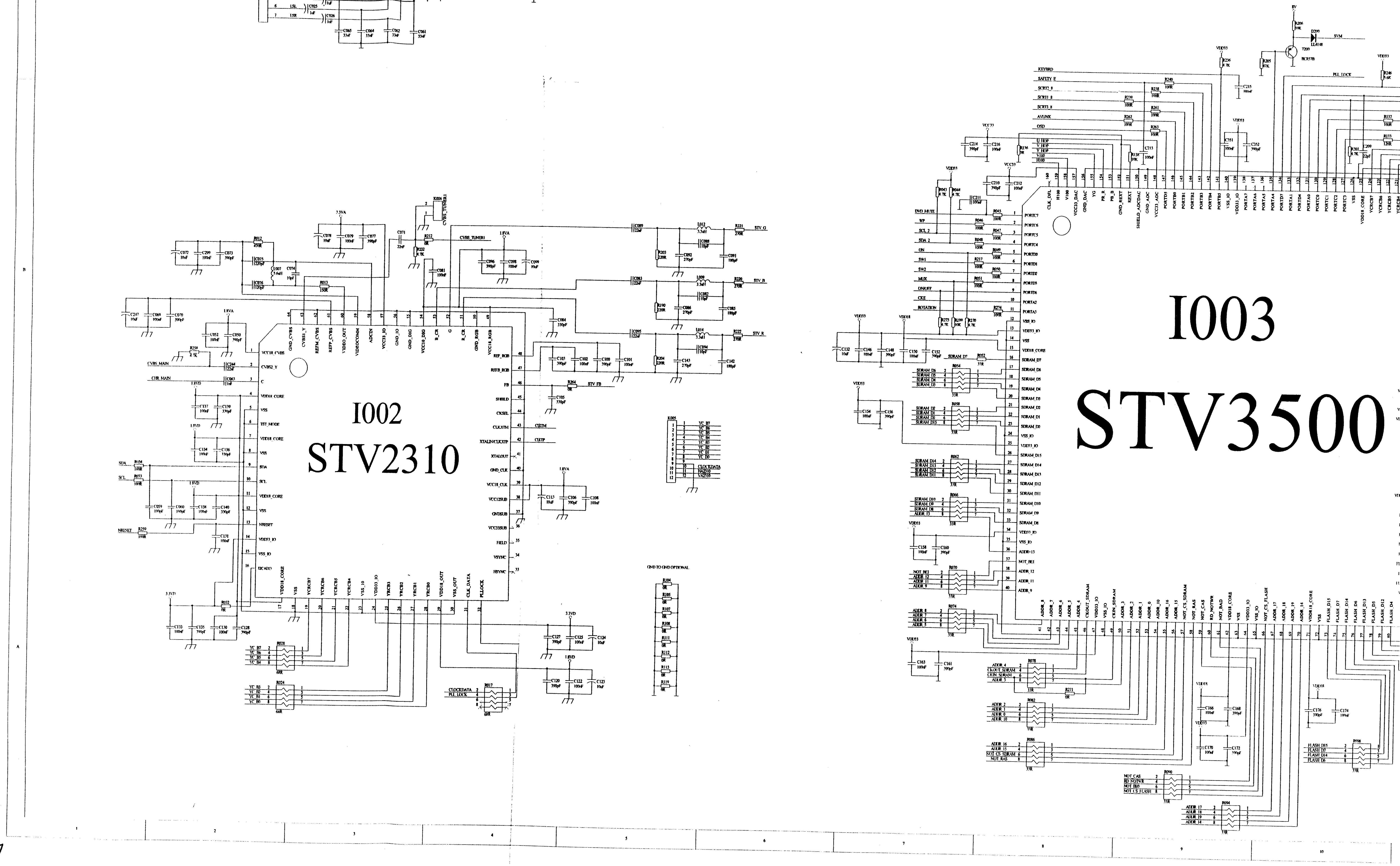
OTHER INFORMATION

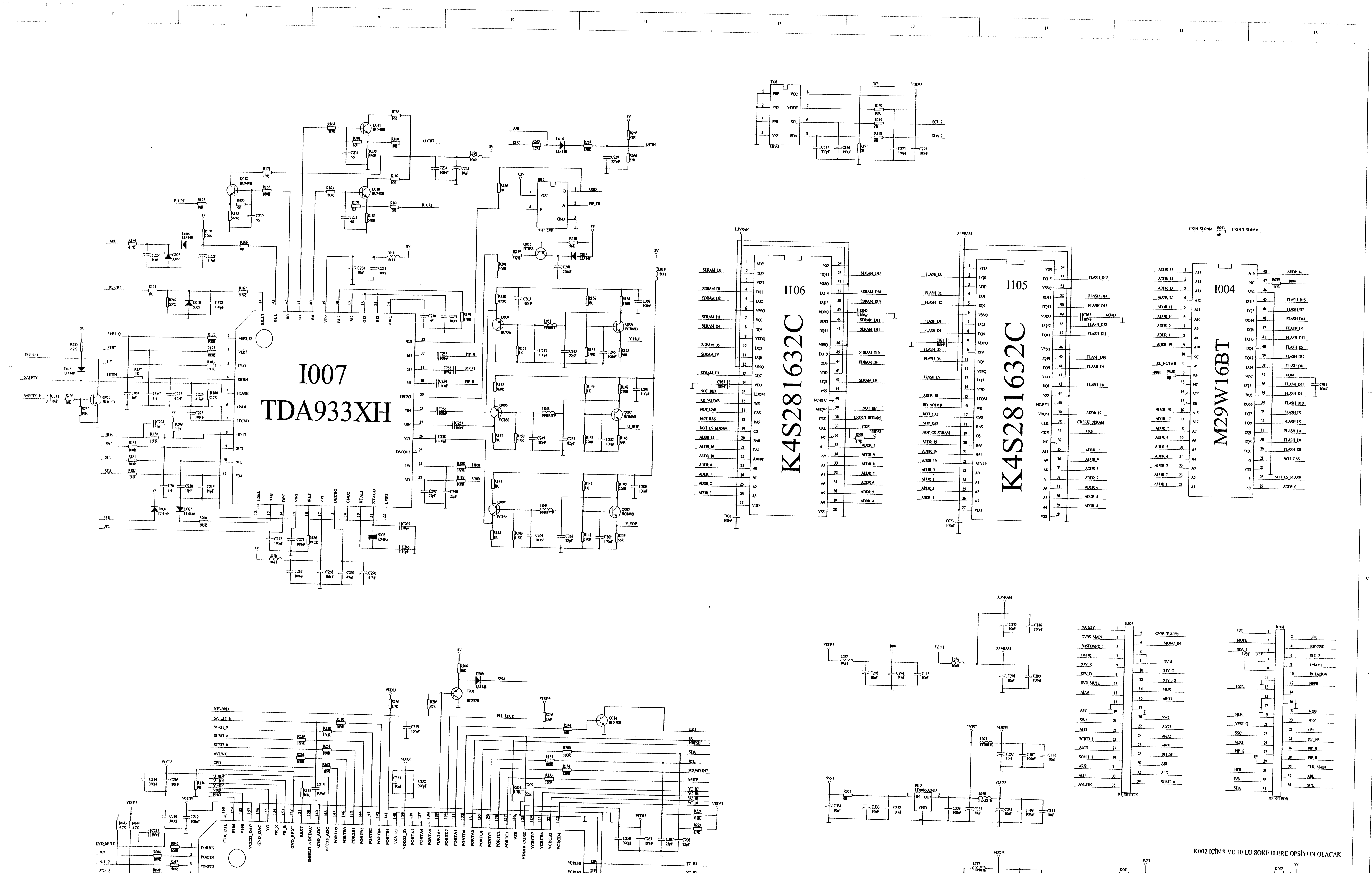
Part Number	Marking	Weight	Base quantity	Packing mode
BTA/BTB06-xxxyz	BTA/BTB06-xxxyz	2.3 g	250	Bulk
BTA/BTB06-xxxyzRG	BTA/BTB06-xxxyz	2.3 g	50	Tube

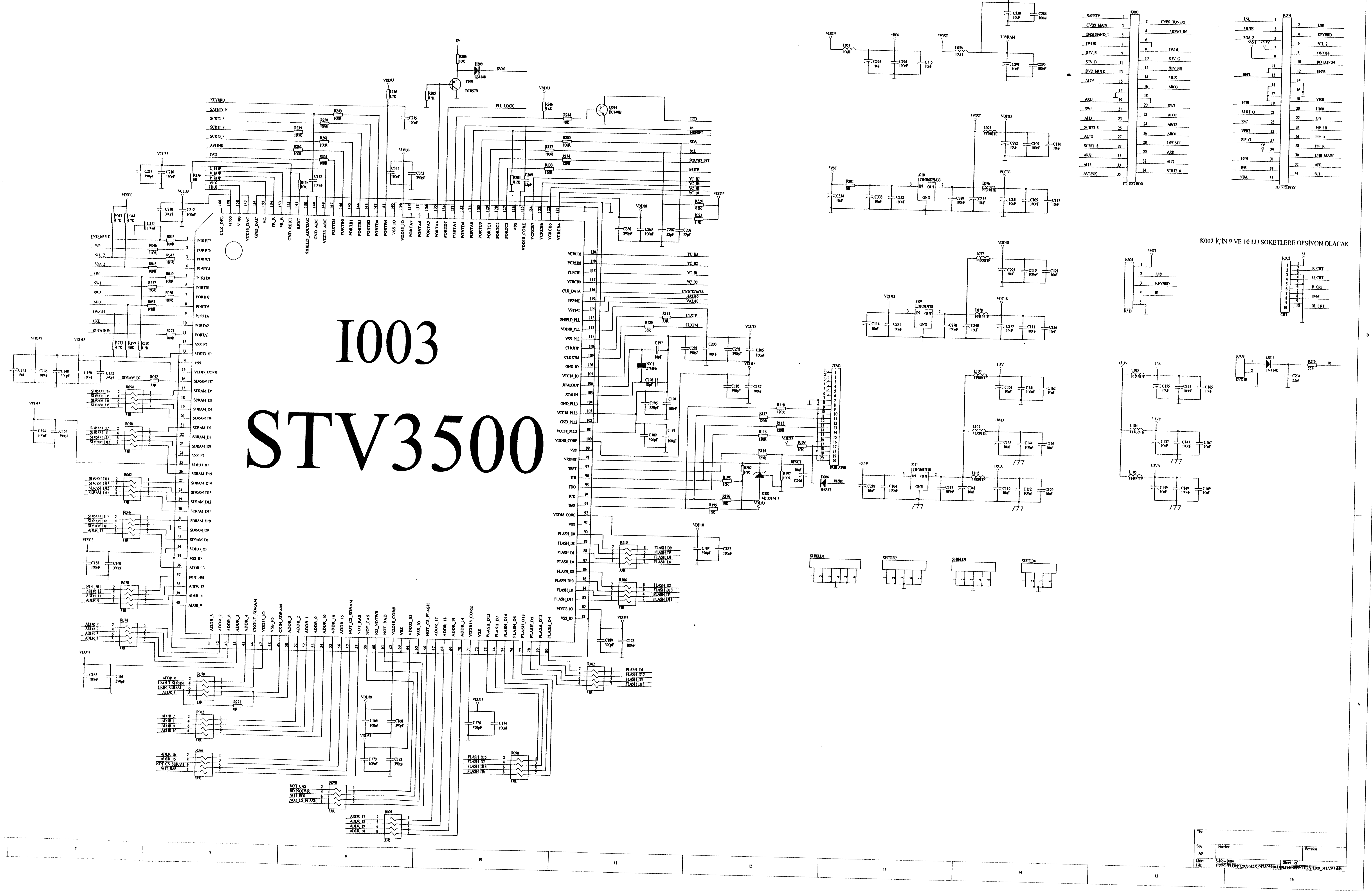
Note: xxx = voltage, y = sensitivity, z = type



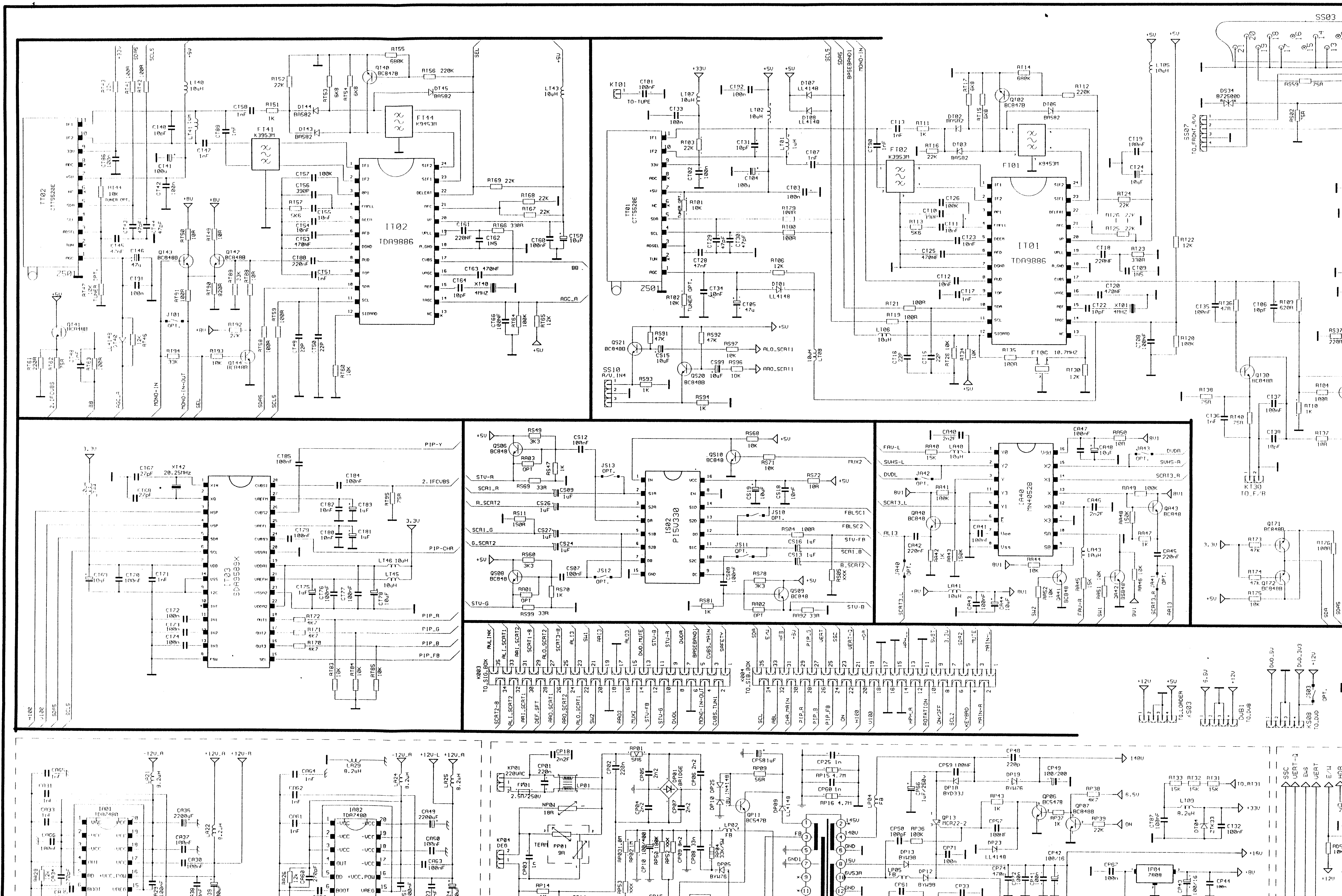
I001
STV82X6
I007
TDA933XH


I002
STV2310
I003
STV3500
STV_G
STV_B
STV_R
STV_FB
GND TO GND OPTIONAL
1
2
3
4
5
6
7
8
9
10
1

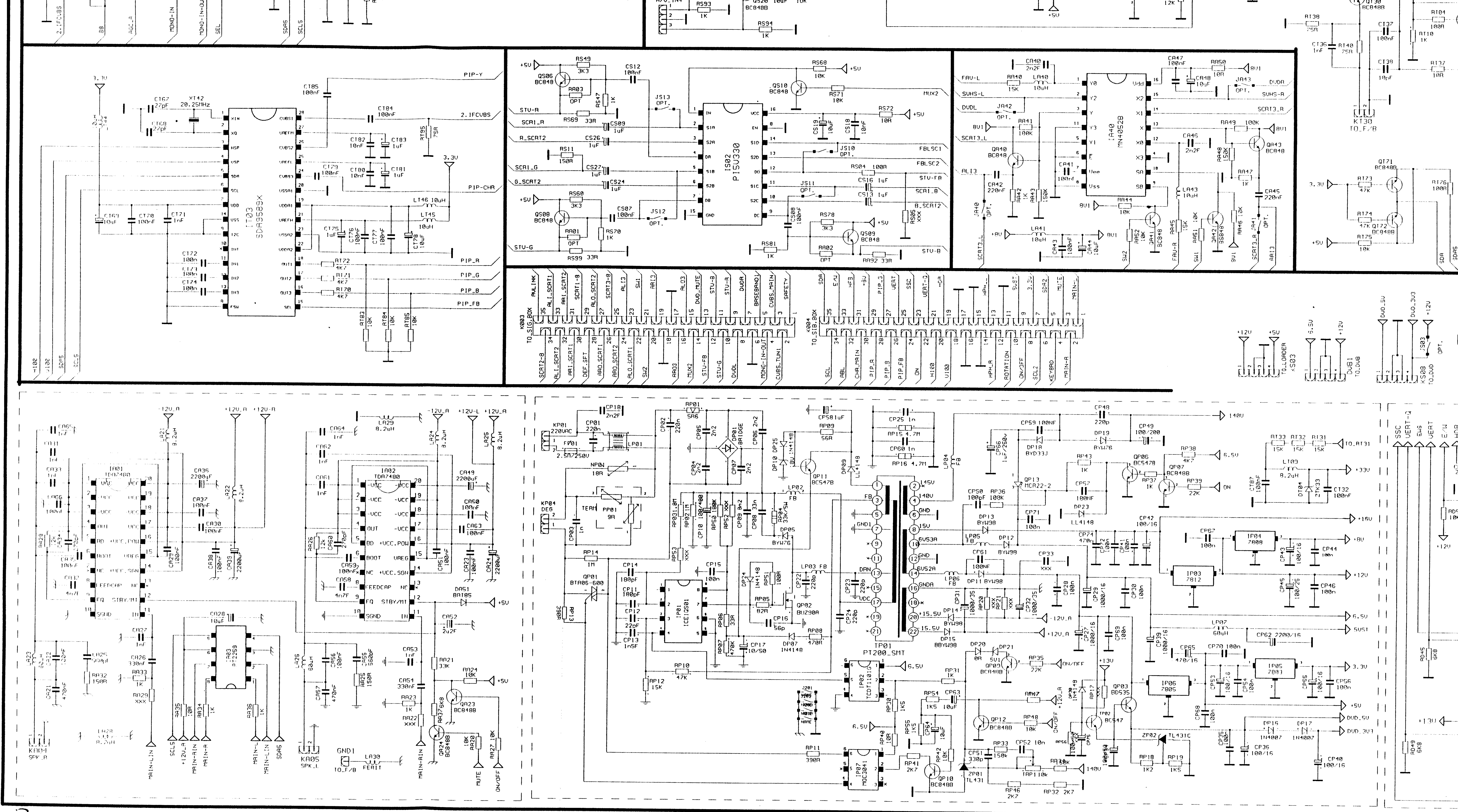

I007
TDA933XH
I106
K4S281632C
I105
K4S281632C
I004
M29W16BT
K002 İÇİN 9 VE 10 LU SOKETLERE OPSİYON OLACAK

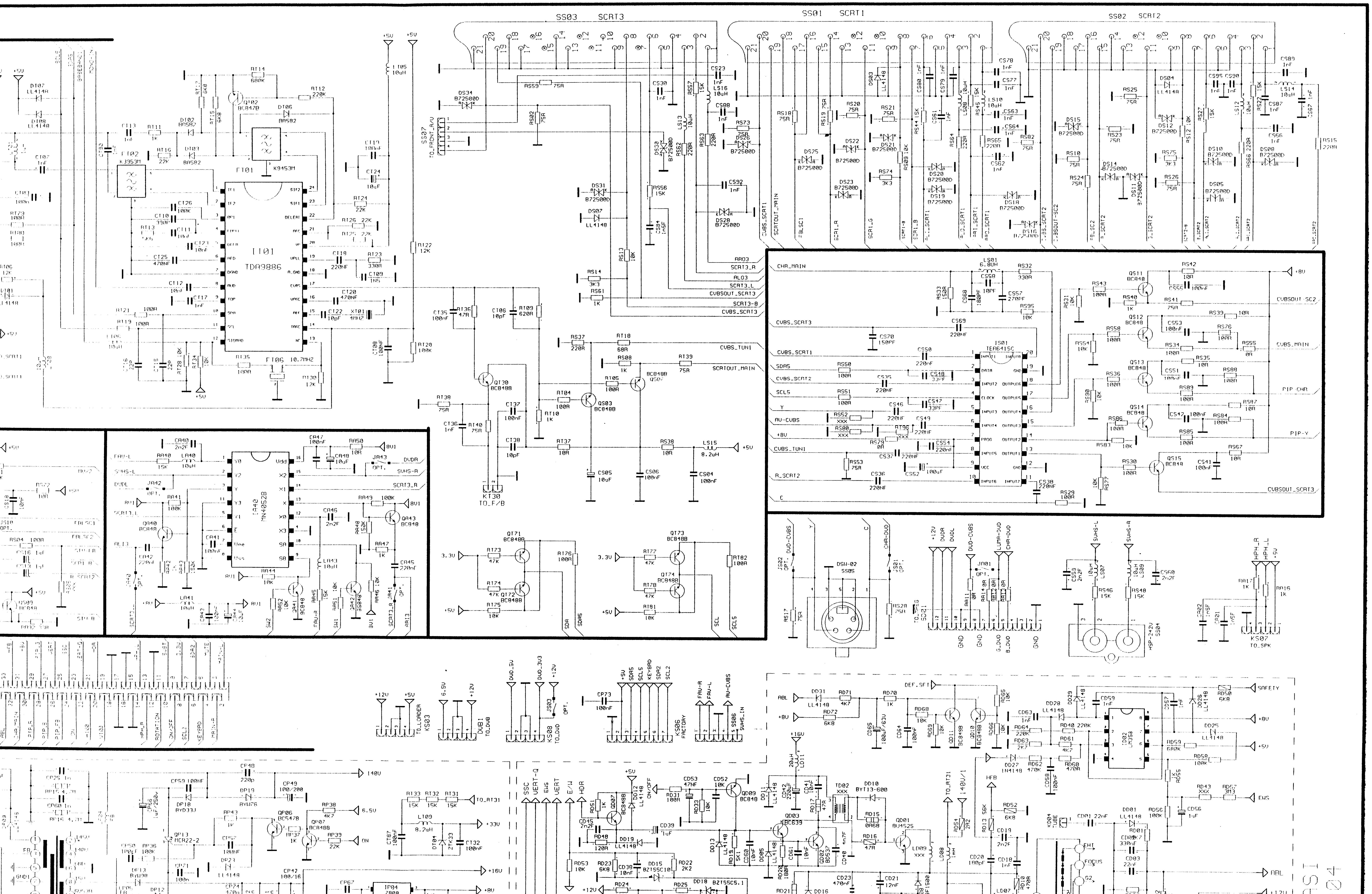


2

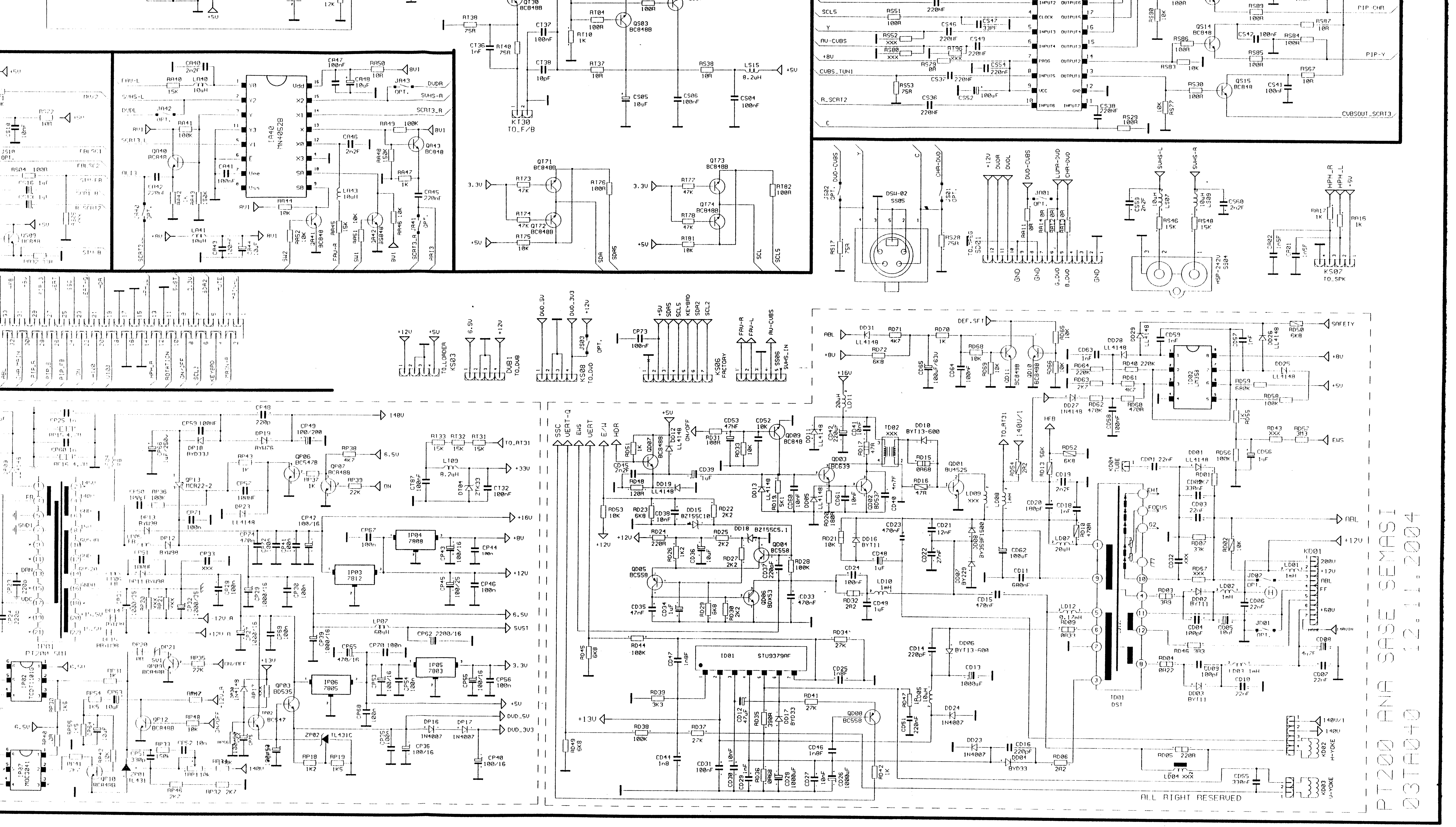


SS03
IT02
TDA9886
IT01
TDA9886
IT03
SDA9389X
IS02
PI5V330
IA40
MN4052B
IA01
TDA7480
IA02
TDA7480
FI41
K3953M
FI44
K9453M
FI02
K3953M
FI01
K9453M
TT02
TT01
Z501
KI01
TO-TUPE
SS10
A/V_IN4
SS07
TO_FRONT_A/V
KI30
TO_F/B
K003
TO_SIG.BOX
K004
TO_SIB.BOX
XS03
TO_LOADER
DVB1
TO.DVB
KS08
TO.DVD
KP01
220VAC
KP04
DEG
PIP-Y
2.IFCVBS
PIP-CHA
PIP_R
PIP_G
PIP_B
PIP_FB
AGC_A
BB
SEL
SDA5
SCL5
MONO-IN
MONO-IN-OUT
BASEBAND1
ALO_SCRT1
ARO_SCRT1
MUX2
FBLSC1
FBLSC2
STV-FB
SCRT1_B
B_SCRT2
STV-B
STV-R
SCRT1_R
R_SCRT2
SCRT1_G
G_SCRT2
STV-G
FAV-L
SVHS-L
DVDL
SCRT3_L
DVDR
SVHS-R
SCRT3_R
140V
+33V
+15V
+8V
6.5V
ON
IO_RI31
SSC
VERT-Q
EWS
VERT


IT03 SDA9589X
X142 20.25MHz
IS02 PI5V330
IA40 MN4052B
K003 TO_SIG_BOX
K004 TO_SIB_BOX
IA01 TDA7480
IA02 TDA7480
IA03 AT2569
IP01 ICE1QS01
TP01 PT200_SMT
IP02 TCDT1101G
IP07 MOC3041
IP03 7812
IP04 7808
IP05 7803
IP06 7805
DP01 BRIDGE
QP02 BUZ90A
QP01 BTA06-600
QP03 BD535
ZP01 TL431
ZP02 TL431C
KP01 220VAC
FP01 2.5A/250V
KA01 SPK_R
KA05 SPK_L
GND1 TO_F/B
K130 TO_F/B
XS03 TO_LOADER
DVB1 TO_DVB
XS08 TO_DVD
3



SS03 SCRT3
SS01 SCRT1
SS02 SCRT2
SS07 TO_FRONT_A/V
IT01 TDA9886
FI01 K9453M
FI02 K3953M
IS01 TEA6415C
IA40 MN4052B
KT30 TO_F/B
DSW-02 SS05
KS07 TO_SPK
KS03 TO_LOADER
DU01 TO_DVB
KS08 TO_DVD
KS06 FACTORY
SS06 SVHS_IN
ID02 LM358
CHR_MAIN
CVBS_SCRT3
CVBS_SCRT1
SDAS
CVBS_SCRT2
SCLS
AV-CVBS
CVBS_TUN1
R_SCRT2
CVBSOUT_SC2
CVBS_MAIN
PIP_CHR
PIP_Y
CVBSOUT_SCRT3
CVBS_TUN1
SCRTOUT_MAIN
ARO3
SCRT3_R
ALO3
SCRT3_L
CVBSOUT_SCRT3
SCRT3-B
CVBS_SCRT3
SAFETY
ABL
DEF.SFT
EWS
HFB
SSC
VERT-Q
VERT
E/W
HDR
ON/OFF
TO_RT31


PT200 ANA SASE SEMASI
03TA040 12.11.2004
ALL RIGHT RESERVED
ID01 STV9379AF
IA40 MN4052B
IP04 7808
IP03 7812
IP05 7803
IP06 7805
ID02 LM358
IP02 TCDT1101G
IP27 MOC3041

4

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

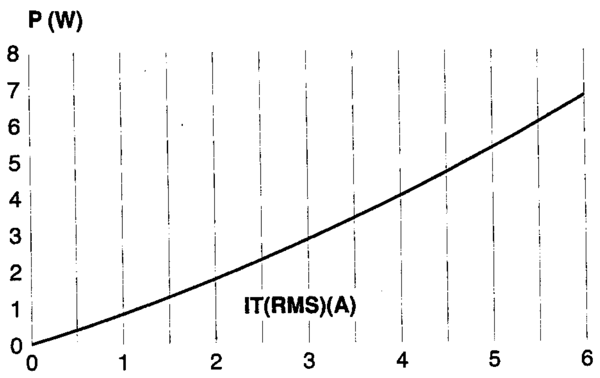


Fig. 2: RMS on-state current versus case temperature (full cycle).

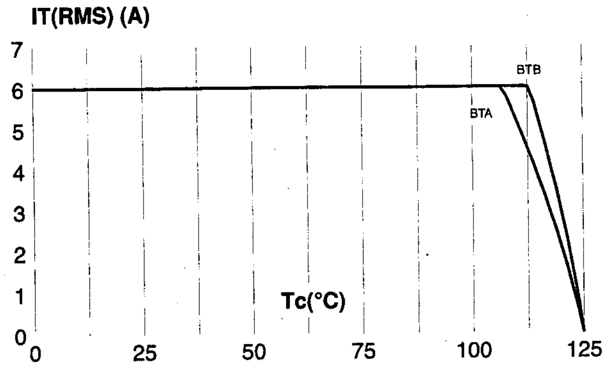


Fig. 3: Relative variation of thermal impedance versus pulse duration.

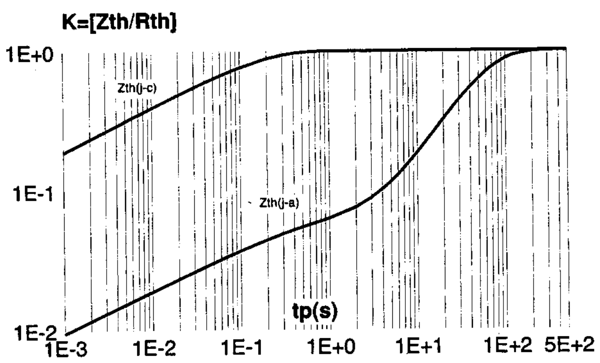


Fig. 4: On-state characteristics (maximum values).

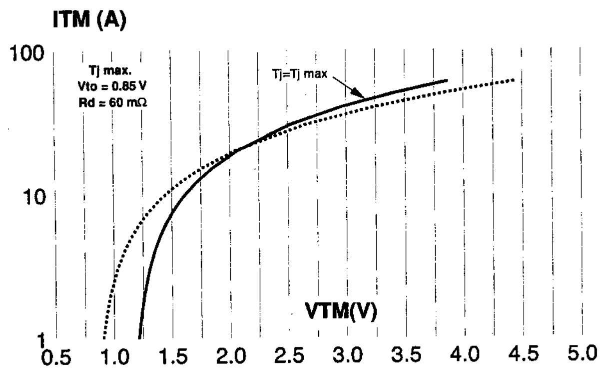


Fig. 5: Surge peak on-state current versus number of cycles.

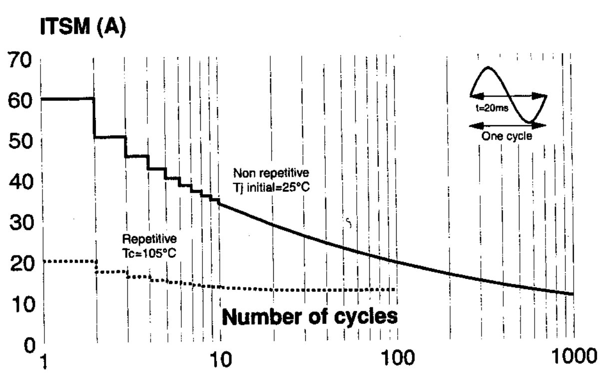


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms, and corresponding value of I²t.

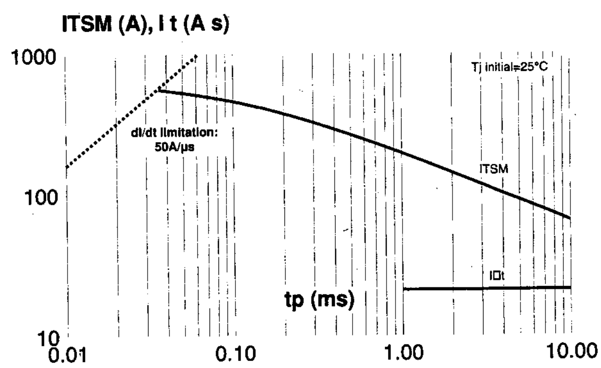


Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

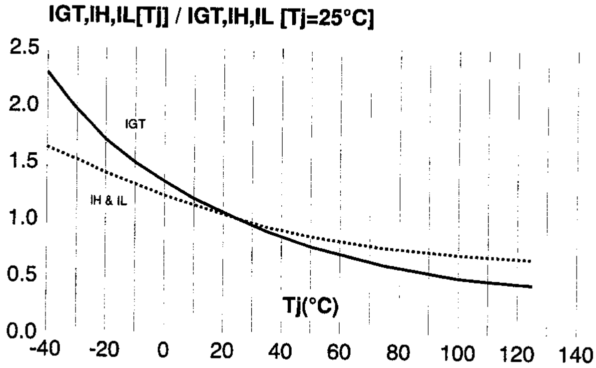


Fig. 8-1: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Snubberless & Logic Level Types

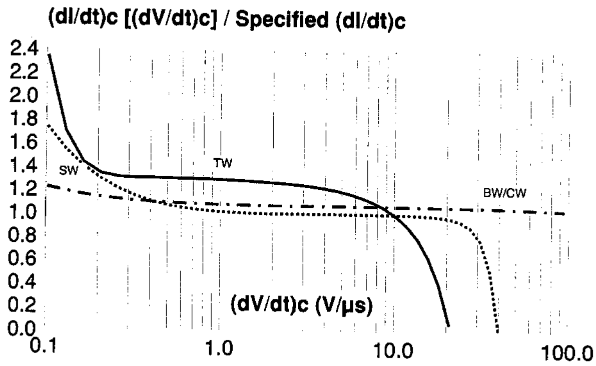


Fig. 8-2: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Standard Types

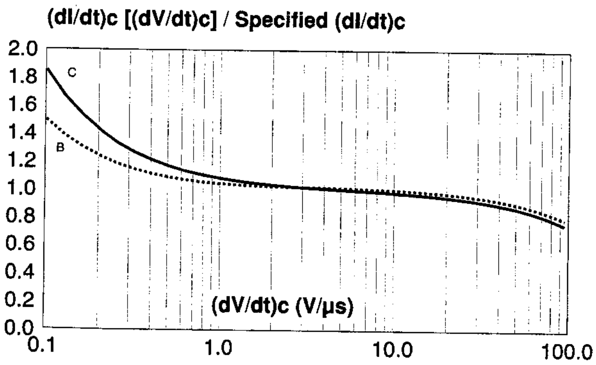


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.